BioPIC - Integration of Biosensors based on Photonic Integrated Circuits by Local-Backside Etching

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ABSTRACT

Silicon photonic sensors are promising candidates for lab-on-a-chip solutions with versatile applications and scalable production prospects using complementary metal-oxide semiconductor (CMOS) fabrication methods. However, the widespread use has been hindered because the sensing area adjoins optical and electrical components making packaging and sensor handling challenging. In this work, a local back-side release of the photonic sensor is employed, enabling a separation of the sensing area from the rest of the chip. This approach allows preserving the compatibility of photonic integrated circuits in the front-end of line and metal interconnects in the back-end of line.

Keywords: Silicon Photonics; Photonic Sensor; Photonic Integrated Circuits; Point-Of-Care-Diagnostics.

1. INTRODUCTION

Silicon-based photonic biosensors integrated into a semiconductor chip technology can lead to significant advances in point-of-care applications, food diagnostics, and environmental monitoring through the rapid and precise analysis of various substances [1]. In recent years, there has been an increasing interest in sensors based on photonic integrated circuits (PIC) because they give rise to cost-effective, scalable and reliable on-chip biosensors for a broad market. The PIC technology employs typically silicon-on-insulator (SOI) wafer, which is the most attractive approach from a commercial point of view since it provides a scalable platform for mass production using complementary metal-oxide semiconductor (CMOS) fabrication processes.
Once the photonic chip is fabricated, it can be used for homogeneous sensing of refractive index variations or it is employed for surface sensing by coating the silicon waveguide with a covalently attached sensing layer. The sensing layer determines the specific detection and, hence, the application. This step, however, is independent of the fabrication of the chip, making the PIC technology based on SOI wafer attractive for both, science and industry. A further advantage of PIC-based biosensors is the possibility to realize sensor arrays using, e.g., an inkjet surface functionalization process. This allows for the detection of several substances in parallel (multiplexing). During the last two decades, integrated photonic sensors have been intensively studied in terms of sensitivity and reliability.
However, the bottle-neck for a transfer from laboratory to industry is the position of the sensing area, since it adjoins optical and electronic components. This prohibits cost-effective packaging and makes the sensor handling impractical. Current photonic sensors based on PIC technologies are interacting with the analyte from the top side of the photonic chip; i.e., the sensor element such as a ring resonator is released by etching through the oxide cladding on top of the SOI waveguide. Here, the light source, sensor and light detector are on the same side of the chip. The most severe problems are the packaging and handling because PIC-based chips are always millimeter-sized, obstructing the integration of electrical interconnects and microfluidics for high-throughput.
Currently, these problems are tackled by enlarging the chip size or by using sophisticated microfluidics or packaging techniques [2]. This dramatically increases costs and prohibits ease of use for the surface functionalization. Further, the front-side release makes a monolithic integration of silicon photonic sensors into a CMOS or SiGe BiCMOS technology challenging due to the complex material stack of the back-end of line (see Fig. 1).

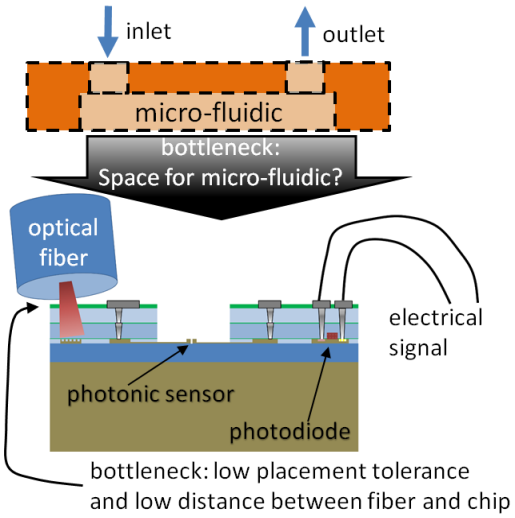

Fig. 1: Current status of optical sensors in a photonic integrated circuit technology. The optical light coupling, connection with micro-fluidics and wafer-level packaging are identified bottlenecks that hinder a mass-production.

In general, silicon photonic sensors need to be sealed, connected to pumping peripherals, and often bear electrical and optical connections.
To tackle this general problem, we developed a novel integration approach to separate the sensing area from the rest of the chip by releasing the silicon photonic sensor from the back-side of the chip. For the first time, this gives perspective to a fully packaged, cost-effective photonic sensor platform that can be monolithically integrated.

2. STATE OF THE ART

Towards disposable sensor chips, the use of a single wavelength light source in combination with a chip-integrated photodiode is preferable since optical spectrum analyser are expensive and cannot be miniaturized currently. As mentioned before, such a configuration can be used for intensity measurements. However, the main drawback of intensity measurement is the small detection range.
Currently, approaches to track the peak position with a laser and photodiode is realized with a tunable laser, which is expensive and requires much space. To avoid this, a tunable optical filter is placed in front of the optical sensor [6]. In this way, a broadband light source such as a superluminescent diode can be used because only certain wavelengths with sharp linewidth can pass the optical filter. The transmitted center wavelength can be tuned, so that the working principle of a tunable laser is achieved. The advantage of a tunable filter is mainly referred to the fact that it can be realized by integrating an additional add-drop ring resonator that is thermally tuned using the relatively large thermo-optical effect in silicon. Metal plates in the back-end of line can be employed as heater.
Another bottleneck is related to the light coupling from the external light source into the chip. Single mode optical fiber having a mode field diameter of 10.4 µm and a numeric aperture of 0.14 are typically used. Due to these characteristics, the optical fiber needs to be placed above chip with a distance of about 3 µm, making the fiber alignment challenging. Therefore, precision 3D translational stages are used.
However, the alignment procedure is too time consuming and the tolerance against misalignment is too small. Current research is focused on the development of cost-effective fiber-to-chip packaging methods to overcome this issue. The optical sensor elements can be co-integrated with light-sources and photodetectors. Even a monolithic integration with electronic devices is possible by using an electronic-photonic-integrated circuit (EPIC) technology.
However, PIC technology has a higher potential for disposable sensor applications since the fabrication is significant cheaper than EPIC. The main bottleneck is still the integration of a light sources. Therefore, optical fiber coupling using on-chip grating coupler is still required. In summary the main bottleneck for cost-effective and reliable sensor integration is the co-integration of light-source (optical fiber), electrical signal supply and micro-fluidic from same interface.

3. BREAKTHROUGH CHARACTER OF THE PROJECT

We propose a novel approach to overcome this general issue. Our integration concept is based on a wafer back-side release that enables a separation of sensing area and, hence, the microfluidic from the optical fiber and electrical contacts. A schematic is shown in Figure 2. As it can be seen from this figure, a second major advantage of this approach is the improved compatibility to the baseline CMOS-process, i.e., the complete back-end of line can be fabricated in a similar way as in the standard

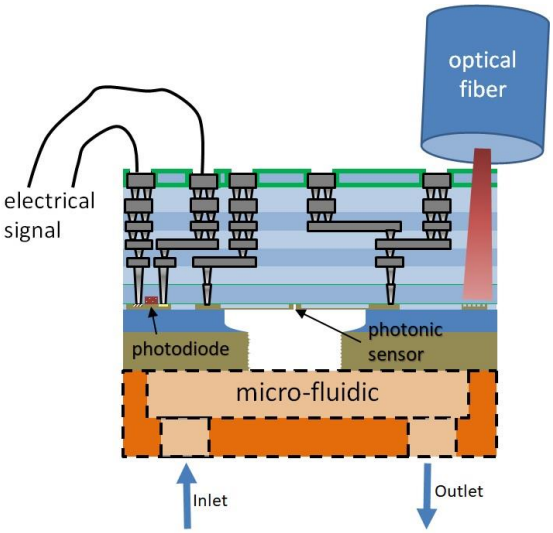

Fig. 2: BioPIC approach: Photonic sensor integration in a photonic integrated circuit technology.

process. For the first time, this gives perspective to a fully packaged, cost-effective photonic sensor platform; ready to use for scientists as well as industrial partners in Europe. This technology is intended to create a "large scale effect", because it enables the development of numerous applications in health-care, food analysis as well as environmental monitoring, which is expected to improve our life quality and gives special benefit to European citizens and civil society in general. Since it has an extremely broad application spectrum it is further expected to trigger innovative start-ups in Europe and to create jobs in different disciplines.

Tab. 1. Comparison of state of the art with the BioPIC solution.

Criteria	State of the art	BioPIC
Fiber alignment tolerance	< 1µm	65µm
Foot print of sensor-chip	>5mm²	<0,5mm²
CMOS-compatibility	medium	high

4. PROJECT RESULTS

In principle, the photonic sensor is released by a local back-side dry-etch followed by a combination of different chemical wet etch processes. The project BioPIC aims to develop this technology on wafer-level for a scalable fabrication of photonic sensors. The fabrication is done by utilizing a PIC-technology at IHP, Germany. This technology employs 200 mm silicon-on-insulator wafer having a 2 µm buried oxide and a 220 nm crystalline silicon layer on top. A 248 nm DUV optical lithography is used to define the waveguide structures. Then, the chip is fabricated, including all five metal stacks in the back-end of line. To protect the back-end of line against the relatively long etching time and to enable a back-side integration on wafer-level, the passivation of

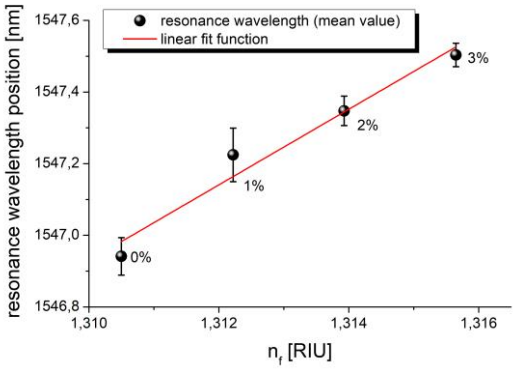

Fig. 3: Optical spectrum of the back-side released micro-ring resonator. Adopted from Ref. [7].

the top metal pads is modified following the procedure reported in [3]. This is required because the ring resonator is released by a deep silicon etch followed by a chemical wet etch. As a consequence, the wet etch would underetch the standard passivation and, hence, destroy the metal pads. The adjusted passivation based on a flattened silicon nitride layer has been proven to protect the back-end of line. A detailed description of the fabrication process with focus on the back-side release process is provided in [4].

To test the viability of the fabricated photonic sensor, we perform a homogeneous sensing experiment to evaluate the sensitivity. Developing application-specific sensors is typically a balancing act between sensitivity and optical losses traded off against each other within the limitations of the present fabrication flow. On the one hand, narrowing the line width (FWHM) reduces the detection limit. This can be achieved by lowering optical losses within the ring resonator. On the other hand, lower losses are primary observed through strong confinement inside the silicon waveguide, which leads to a lower interaction with the fluid. As a consequence, the ring resonator sensitivity is reduced at the same time.

One strategy to find a trade-off is the use of a partially slotted ring resonator [5]. This approach combines a rib waveguide with a slot waveguide. The slot waveguide exhibits higher optical losses, which are caused by random line-edge sidewall roughness scattering. However, its high sensitivity makes it suitable for sensing applications. Here, we use a rib waveguide and a strip-loaded slot waveguide.

The ring resonator is located in the middle of the LBE area. A racetrack configuration is used to introduce the slot waveguide within the straight part of the ring. The silicon strip loads are necessary to avoid an over etch of the silicon waveguide and are used as etch stop. We inferred an extinction ratio of 20 dB and a full width at half maximum of 0.55 nm from the observed optical spectrum of the ring resonator. The sample is fixed on a hot plate in this experiment, and by tuning the temperature, we have revealed a temperature sensitivity of 92 pm/K, which is comparable with a similar ring resonator that has been opened from the top [6]. As proof of principle, we have performed homogeneous sensing

Fig. 4: Silicon photonic sensor chip with packaged with microfluidic.

experiments with different concentrations of NaCl in DI water.
For this experiment, we employed a super luminescence diode and an optical spectrum analyzer with a wavelength resolution of 30 pm, while the photonic chip is fixed on a 3D-printed sample holder with a fluid reservoir. The grating coupler is TE-polarization selective and were used in order to couple the light from a single-mode fiber into the chip. TE-mode operation is achieved by maximizing the output signal through a paddle-style fiber polarization controller.
Liquids with a different weight percentage of NaCl ranging from 0wt\% to 3wt% were dropped onto the silicon photonic sensor using a pipette. To characterize the homogeneous sensing, we plotted the resonance wavelength as a function of the refractive index of the fluid (NaCl in DI water) in Fig. 3. Through a linear regression, we have deduced a ring resonator sensitivity of 106 nm/RIU, which is comparable with values reported for similar micro-ring resonators released from the front-side [6].
Finally, a simple and cost-effective micro-fluidic was developed by taking advantage of the back-side released photonic sensor. In this case, only two holes in a plate are necessary because the LBE window itself is acting as fluidic channel. In this way, we can ease the fabrication of microfluidics and reduce costs drastically. Fig. 4 shows a photonic sensor chip packed with such a microfluidic.
In conclusion, the proposed local back-side release photonic sensor platform opens a new route towards high-throughput packaging because the optical and electrical interconnects are on the same side of the chip, while the fluidic can be easily introduced from the opposite side. Moreover, it allows a monolithic integration of photonic sensors, optoelectronic as well as electronic components on the same chip because the back-end of line is completely accessible.

5. FUTURE PROJECT VISION

5.1. Technology Scaling

The envisioned technology can be scaled up by a novel wafer-scale fabrication flow. Currently, the fabrication of photonic sensor chips is done on wafer-level but the fabrication and packaging of the microfluidic as well as the surface functionalisation is realized on chip-level. This makes the complete fabrication flow expensive and hinders a mass fabrication of photonic sensors and make them unsuitable for low-cost applications, were disposable chips are required.
Therefore, we envision a fabrication flow that takes advantage of the back-side released photonic sensor, that was realized in ATTRACT Phase 1. In this case, the chips are fabricated on 200 mm wafer and the surface functionalization will be done on wafer-level by, for example, a layer by layer technique. The microfluidic is connected then connected before the chips are diced. The local-backside release makes this approach feasible because the wafer backside is easily accessible and optical and electrical connection from the upper side of the wafer are not affected.

5.2. Project Synergies and Outreach

Our main idea is to develop for the first time a wafer-scale fabrication flow. In this case, the sensor-chips are fabricated on 200mm wafer. To overcome the bottle-neck of single chip preparation, we aim to develop a wafer-scale surface functionalization. This step requires a company that works with the layer by layer technique. This will be followed by bonding a micro-fluidic on top of the wafer. The microfluidic should be fabricated from a company working in this field. Finally, the wafer can be diced and assembled to a substrate.
In order to address a real world application, the chip will be connected to an electronic readout which requires software and hardware development. For secure data transfer, we need to collaborate with experts in this field.
In summary, to realize our project, we would like to partner with SMEs for the surface functionalization, micro-fluidic fabrication as well as software and hardware development. In this way, we can guarantee a complete fabrication flow, so that science and industry get access to our technology.
Since some steps are identically required for other sensor systems, we can imagine to cluster with similar ATTRACT Phase 1 projects. The same holds for the surface functionalization. Here, we would like to collaborate with ATTRACT Phase 1 projects that may have developed biosensors and can provide us the surface functionalization procedure to run the test on our platform. Based on our ATTRACT Phase 1 experience we are convinced to have highest public dissemination of our results by reporting on them in social media platforms and making short video clips.

5.3. Technology application and demonstration cases

As application that addresses needs of society, science and industry – that has a very recent and immediate effect on all of us, we are planning to develop a Covid-19 antibody test. The main six advantages of the envisioned technology for this application are as follows:

1. miniaturized and mobile sensor plattform
2. rapid results <60sec („Drive-In“ scenario)
3. reliable and secure data transfer
4. digital analysis to avoid bias
5. potential for mass production
6. potential for multiplexing

The final goal of ATTRACT Phase 2 is the demonstration of TRL 7, i.e. a system prototype demonstration in operational environment.

Since our photonic integrated circuit technology is currently offered through the European multi-project wafer platform EUROPRACTICE, we would like to offer the envisioned sensor technology on the same way. In this way we can offer affordable and easy access to our technology. This makes chip design and manufacturing more accessible by providing reduced entry costs, initial advice and ongoing support.

5.4. Technology commercialization

The point-of-care-solution enabled by our technology has the potential for a start-up. The start-up could develop point-of-care-solutions but also it can provide a market to sell photonic biosensors to scientific institutions. Therefore, we would start to contact investors during ATTRACT Phase 2 in order to realize such a start-up. Since such an interdisciplinary topic has a plenty room of space for innovations/applications that can be transferred to market, we would also apply for other funding sources during phase 2, especially to get funding for the aforementioned start-up.

5.5. Envisioned risks

The main risk of a potential phase 2 project is the yield of fabrication. We aim to provide cost-effective photonic sensor chips but this requires a high yield in fabrication. To achieve this, we will tackle fabrication issues with optimized chip designs.

5.6. Liaison with Student Teams and Socio-Economic Study

In ATTRACT Phase 1 we have collaborated with MSc. Level students from the Technische Hochschule Wildau. This collaboration will be continued and expanded in ATTRACT Phase 2 by initiating a young research group led by the project leader Patrick Steglich. He is scientist at IHP and lecturer for photonics at Technische Hochschule Wildau. Special emphasize will be put on the realization of different sensor prototypes, that will be realized by the students in terms of a contest. Besides that, we will contribute with interviews, short video clips and technology impact references to the expert-driven socio-economic study of the ATTRACT initiative and ecosystem.

6. ACKNOWLEDGEMENT

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