DIBIS, a Digital Burst Image Sensor with a High Dynamic Range High Speed Pixel Operating at 100 Million Frames Per Second

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ABSTRACT

CMOS Image Sensors are widely employed in the study of high-speed phenomena such as high-energy physics, micromechanics or explosives. Unfortunately, these suffer from a limited input/output rate and a limited dynamic range. In this project, we use the burst imaging concept, which consists in a dedicated architecture that stores the video frames within the sensor and it enables a pixel rate of about 1 Terapixel per second. In addition, we also propose a novel pixel design that is able to operate at this speed with high dynamic range features. In this paper, preliminary results of a 2D demonstrator are presented and an architecture of the digital burst image sensor based on a 3D stack of three CMOS wafers with a storage in the digital domain is proposed. Results show that the pixel frontend can operate at 100 Mega frames per second with a high dynamic range feature. In the DIBIS project Phase 2 we plan to create a European ecosystem for high speed image sensors and to manufacture the sensor in a 3D stacked technology.

Keywords: High-speed imaging, CMOS, video sensor, current mirroring integration, burst imaging

1. INTRODUCTION

High-speed imaging is a key technology to study high-speed phenomena such as micromechanics, explosives, plasma formation mechanisms or laser ablation. The burst imaging concept introduced by Etoh avoids the bottleneck of the data input/output of the sensor by storing the series of images within the sensor [1]. In this way, a pixel rate of about 1 Terapixel per second can be achieved while the conventional approach that extracts continuously the frames from the sensor is limited to a few tens of Gigapixel per second [2]. Thus, a frame rate of several Megaframe per second (Mfps) can be achieved with a spatial resolution of about 1 Megapixel [3] and a frame rate of several Gigaframe per second (Gfps) has been demonstrated with a streak camera approach with a reduced spatial resolution [6]. At such a frame rate, the exposure time is limited, thus the pixel analogue front end must operate at a high speed while providing a high gain.

The concept of storing the pixel within the sensor is relevant in the framework of a 3D stacked integrated circuit approach. Indeed, storing the images in an additional tier allows to save space on the first one that could be utterly dedicated to the sensitive part of the pixel to increase the fill factor. Additionally, the supplementary tier allows storing more frame in order to increase the movie length. Moreover, pushing the 3D stacked up to 3 or more tiers makes it possible to implement more on chip functionality such as analogue to digital conversion [5][6] or even implementing artificial intelligence functionalities.

The paper describes an architecture of a burst image sensor (BIS) dedicated to a 3D stack of 3 integrated circuits with on-the-fly digitalization and embedded digital storage. A 2D monolithic demonstrator integrating the different electronic parts of the sensor side by side has been designed in a 65 nm CMOS technology. The design of a novel high dynamic range (HDR) pixel front-end suitable for 3D integration is also presented.

2. STATE OF THE ART

Most of the BIS are designed with CCD and a few with CMOS technology. The CCD based sensor maximal frame rate is limited to about 10 Mfps by the charge transfer which is a slow process[3]. The CMOS technology operating with voltage instead of charge transfer allows to reach a higher frame rate of 100 Mfps [7] or even almost 10 Gfps with a streak imaging paradigm[4].

All the current BIS are designed with a 2D monolithic sensor and, as a consequence, have a limited number of

frames stored inside the pixel to about 100 up to 300 frames even with a large pixel pitch of about 30 to 40 µm. The spatial resolution is thus restricted to less than 1 Megapixel. Only 3 commercial products are currently available on the market based on the sensors presented in Table I. Moreover, all the current designs store the frame in the analogue domain in a CCD register or a capacitance and it is well known that this type of memory is not reliable.

Two very first prototypes of digital BIS with on-the-fly analogue-to-digital converter have been already designed by the authors [5][11][6]. The first one was designed with a stack of 2 CMOS chips with a simple ramp ADC and the second one was a demonstrator aimed for the current sensor proposal with 3 tiers described in the next section.

3. BREAKTHROUGH CHARACTER OF THE PROJECT

The proposed sensor is a breakthrough with respect to the state of the art. Whereas all the currently available BIS are using analogue memory cell such as CMOS capacitances or CCD registers, the new proposed BIS will use digital memory cell. Although the digital approach implies a more complex design, it offers several decisive advantages with regards to the analogue one. In fact, the digital storage offers a better data reliability inside the sensor, especially in hard experimental environment such as X-ray applications. It can also generate a better image quality as the signal is digitized in the heart of the pixel, thus no additional noise is added. Moreover, the digital domain provides a higher data density in the advanced digital CMOS process. As a consequence, more frames can be embedded within the sensor and it has been demonstrated that more than 500 frames with a 12 bits per pixel resolution can be amassed within a 40×40 µm² pixel with a digital memory realized with a 28 nm digital CMOS process. Additionally, the concept of 3D microelectronic and the digital approach pave the way to the advanced digital processing and to artificial intelligence in the field of ultrafast imaging.

In addition to the advantages of the digital approach, the sensor will also benefit from some new features. A dynamic of 12 bits is expected to be reached thanks to a novel high speed pixel that has already been designed during the phase 1 of the attract project. The proposed pixel offers a HDR feature compatible with the recording of extremely fast moving objects without any blurring effects. The feature is carried out by mirroring in parallel the photocurrent into several integration capacitances before the digitalization of the corresponding frame. The output is automatically selected by the pixel and an additional bit indicates the selected gain.

The sensor architecture is based on a cluster of the pixel sharing the same ADC. Thus, to achieve a frame rate of 10 Mfps, the ADC has to sample at 100 Ms/s to digitalize a cluster of 10 pixels. This architecture offers a powerful programmable binning feature that allows to increase the frame rate by trading off the number of pixels to read out from the cluster. In this way, with a frame rate of 10 Mfps at the full spatial resolution, a frame rate of 20 Mfps can be achieved by reducing the resolution of a factor two, thereby doubling the number of frames that can be stored in the memory.

In conclusion, the targeted performance of the sensor are depicted in Table I and are compared to the available commercial sensors (up to ×20 more rapid, ×4 more dynamic, up to ×5 more pixels, ×2.7 up to ×27 more frames).

Tab. 1. State of the art of high speed burst imagers and the proposed design

	Etoh [10]	Kirana [3]	Etoh [9]	Tochigi [8]	Uhring [4]	DIBIS This Project
Commercial product	yes	yes	no	Yes	no	Aimed to be commercialized during phase 2 of attract
Array size	456×362 (2D)	924×768 (2D)	576×512 (2D)	400×250 (2D)	1×64 (Streak)	600×900 per chip (2D)
Pixel size	66×66 µm²	30×30 µm²	13×13 µm²	32×32 µm²	26 µm	40×40 µm²
Frames	117	180	10	128	128	>500 up to 5000 (reduced resolution)
Dynamic	10bits	10bits	10 bits	10bitst	9 bits	12 bits
Storage	Analog	Analog	Analog	Analog	Analog	Digital
frame per second (fps)	16 M	5 M	100M	5M (full frame) 10M half resolution	8 G	10M (full resolution) 100M (reduced resolution)
Technology	CCD BSI	CCD Microlense	CMOS 0.13µm	CMOS 0.18 µm	BiCMOS 0.35 µm	Heterogeneous CMOS 90 nm, 40 nm, 28nm

4. PROJECT RESULTS

The overall description of the sensor is presented in Fig. 1. The 3D design allows a better repartition of the electronic part. A first IC is dedicated to the analog pixel array. A second one is devoted to the ADC and the last one is dedicated to the embedded digital memory. The main targeted specifications are 600×900 pixels with a pixel pitch of 40 µm, 10 Mfps at full frame resolution, a dynamic of 12 bits and a memory of more than 1000 frames. As the I/O of the sensor can be placed to its bottom side, if a compliant topology is adopted, i.e. the surface of the 3 chips are equal, the sensor is borderless and thus can be assembled side by side to form an optimized lattice that increases the resolution. For instance, a lattice of 2×2 sensors with a 600×900 individual resolution leads to a total resolution of 1200×1800 pixels.

The straightforward implementation of this architecture utilizes an ADC and its associated memory for each pixel as almost all of the existing BIS use a one-to-one connection to the pixel, i.e. a memory bank dedicated to each pixel. However, such topology is not necessarily optimal in terms of sequence depth, i.e. the number of storable images, and in terms of frame rate. An approach with cluster of pixels sharing the same memory unit adds an interesting feature of memory length and frame rate improvement at the cost of spatial resolution. This line has been recently used with a 3D stacked global-shutter image sensor [8]. In addition, targeting an on-the-fly analog-to-digital conversion at a targeted frame rate of several tens of Mfps requires a high speed ADC which results in a large silicon area occupation and a high power consumption. Likewise, segmenting the floorplan of the memory to a unit for each pixel is not optimal in terms of memory capacity. For all these reasons, a cluster approach has been adopted for the BIS. The detailed architecture of the sensor according to the different tiers is shown in Fig. 1.

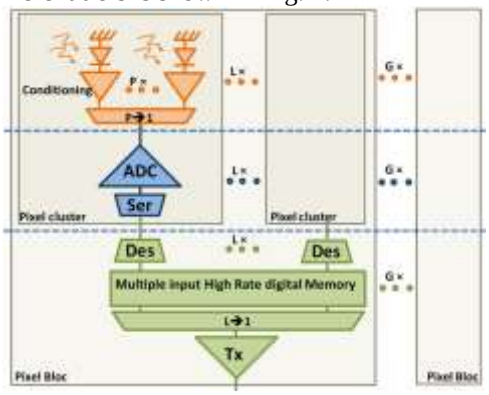

Fig. 1. Detailed architecture of the sensor split in the different tiers. A pixel cluster is composed of P front-end pixels connected to one ADC. A block of L clusters shares the same digital memory.

A cluster of pixels is composed of P=10 frontend pixels connected to one ADC. A block of L=4 clusters, i.e. LxP pixels, shares the same digital memory for an optimal floorplan configuration that allows embedding the maximal amount of memory. With an ADC operating at a sampling rate Fs, the achievable frame rate is therefore Fs/P in the "full frame" mode that consists in reading all the pixels of the cluster. However, the cluster approach adds an innovative feature in burst Imaging. By assuming a constant data conversion rate, the frame rate increases as the number of read pixels in the cluster is reduced and can be written as (1):

$$Fps = \frac{Fs}{P} \cdot \frac{P}{P_{RC}} = \frac{Fs}{P_{RC}} \qquad (1)$$

where P is the number of pixels in the cluster and $P_{RC} \in [1;P]$ is the number of read pixels within the cluster. Likewise, the movie length is also increased by a factor P/P_{RC}. Increasing the frame rate is interesting in high speed imaging to detect faster events whereas expanding the movie length allows the observations of fast and complex events that last for a longer time. While using this feature, the ADC and memory efforts are kept constant whereas the pixel front-end operates at a higher speed. Thus, the front-end bandwidth must be high enough to operate at the highest frame rate or it must be increased as the frame rate increases to keep the sensor sensitivity constant.

A previous work consisting in a 2D monolithic demonstrator is depicted in Fig. 2 and shows that this architecture is doable with performance close to the above mentioned targeted specification [6]. Experimental results show that the proposed structure is fully functional, and can operate at the frame rate of 5 Mfps. The used cluster approach allows to trade off the frame rate and the spatial resolution. The novel HDR pixel [11][12] simulation results show that a dynamic range of 12 bit can be obtained at a frame rate of 100 Mfps. The 2D demonstrator in combination with the novel pixel architecture study of Phase 1 paved the way to the very first 3D stacked BIS with digital storage.

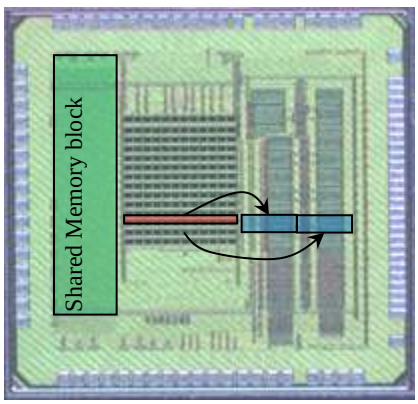

Fig. 2. Previous work demonstrator die photography. Highlighted: two clusters of 10 pixel (orange) and their two associated ADCs (blue) and the shared memory bank for the block of 12 digital clusters (green).

5. FUTURE PROJECT VISION

Despite the disruption of COVID-19, the CIS market stands up with an increase of 7% on a year-on-year comparison [13] mainly driven by medical, aerospace and defence industries. This is a strong indicator of resilience and of the need to continue improving on the CIS technology development.

While the Phase 1 of the Attract project mainly consisted in a technology demonstrator and a feasibility study, in preparation for Phase 2 we are building a stronger European industrial and academic consortium with mixed experience and expertise to address the challenges of realizing a manufactured 3D stacked ultra-fast imager. Unfortunately, at this stage, only a few companies, i.e. Sony using probably a TSMC process [14], provides a commercially available 3D stacked technology employing 3 layers.

When it comes to the European scene, a few companies offer 2 layer stacking (for example ST Microelectronics or LFoundry) in addition to research centres that have been developing in-house solutions. Moreover, from the discussions with potential European partners in design, there is also a strong interest towards CIS stacking with more than 15 companies across different expressing interest for the project. In addition, from preliminary discussions with the ESRF, a DIBIS sensor targeted for X-Ray applications would be an ideal candidate for utilisation in physics experiments.

We believe that the combination of application requirements for fast imaging in combination with the technological challenges to build a European 3D stacked sensor make DIBIS the ideal project to build further European expertise and know-how in semiconductor imaging.

5.1. Technology Scaling

During the execution of previous work, we have demonstrated TRL 3 for the system and TRL 4 for sub blocks of the system. In Phase 2, we plan to move to TRL 6 and prove that the technology can work in operational conditions. We are confident that such a goal can be achieved as we have already proven the design validity and where possible we plan to use commercially available semiconductor technology to manufacture the silicon wafers. The manufactured wafers will have a high level of TRL as it is, by definition, provided by the foundries. We will employ custom manufacturing techniques of research centres in the consortium to assemble the 3D stacking device and we plan to test the device in relevant application conditions.

5.2. Project Synergies and Outreach

To overcome the challenges of the DIBIS project we plan to expand the consortium to a higher number of partners across Europe and with additional dedicated expertise. We are discussing to bring on-board other consortium members that will help in the different steps of the technology development; however, the agreements are not yet finalised and company names are yet to be disclosed:

1. Camera company with strong expertise in Fast X-ray imaging applications.
2. Large Company with expertise in process.
3. Two SMEs with expertise in analog design (pixel-ADC).
4. SME with expertise in digital design and artificial intelligence
5. Research Institute with expertise in process.
6. Research Institute with expertise in design.

In addition, we are open to discuss potential partnerships and use cases with other ATTRACT Phase organisations and we believe that the ATTRACT conference could be an ideal place to strengthen the partnerships.

During Phase 1, simulation results of the proposed pixel architecture have been published. By moving to Phase 2 we plan to further publish and disseminate knowledge deriving from the ATTRACT consortium. Moreover, we plan to publish not only the experimental results deriving from the project but also the lessons learned from the execution and the coordination of the different aspects of the project.

5.3. Technology application and demonstration cases

After the manufacturing of the DIBIS sensor we plan to build at least two technology demonstration cases. The first for scientific purposes in collaboration with the ESRF (we are actively discussing) to demonstrate the validity of the sensor in high-speed physics applications and the second in industrial applications with the involvement of a consortium partner. Furthermore, we will evaluate the potential employment of the DIBIS sensor and its related technology in medical applications, especially for the detection of X-Ray radiation.

5.4. Technology commercialization

During the execution of Phase 1, we have been discussing with research institutes (such as the ESRF) as well as with commercial industrial companies. The ESRF instrumentation team will closely follow the product development. In addition, we plan to have as a partner in the consortium a camera company for the development of the sensor that would immediately be interested in employing these sensors in commercial cameras. In addition, with the know-how and expertise resulting from the execution of the project we plan on designing and offering a family of products for ultra-fast imaging with trade-offs between price and performance. Further work on the commercialisation will be conducted once all the partner of the consortium will be confirmed.

5.5. Envisioned risks

While many risks have been mitigated by previous work and simulations a few key risks are still present. Design: When designing a complex system with multiple wafers, the risk of the design mistakes is present. It can be mitigated with a strong architecture phase and with commercially available simulation tools. 3D stacking manufacturing: the risk of a failure in manufacturing can be high. When stacking multiple wafers, the process yield required for each wafer is multiplied. Moreover, additional yield loss is present when stacking wafers with custom manufacturing techniques. We plan to manufacture multiple wafers to have enough working devices to prove the technology and improve the future manufacturing yield. Thermal issues: by stacking multiple wafers on top of each other, the thermal dissipation becomes a challenge. A novel very low power dissipation concept must be used for the ADC level. A dedicated thermal simulation will be conducted to explore the effect of stacking and to avoid increase of dark current in the pixel array due to the thermal leakage.

5.6. Liaison with Student Teams and Socio-Economic Study

As a University main coordinator, we have access to a high number of MSc. students. Unfortunately, during Phase 1, the COVID disruption made difficult to collaborate with the students, however, in Phase 2, we will work with a team of MSc. students from the Universities of Strasbourg and Grenoble as well as from other consortium partners that would like to be involved. We will organise joint brainstorming sessions guided by an expert facilitator to address Societal Challenges and provide ideas and prototypes inspired to the DIBIS project. Ideally, the facilitator will be a PhD student directly involved in the DIBIS project guided by a senior member coming from an industrial partner of the consortium. A short leaflet of the technology will be provided, and an innovation and creativity course will precede the activities to get the student prepared to the task. With regards to the expert-driven socio-economic study of the ATTRACT initiative and ecosystem we will contribute with dedicated time from industry experts in the consortium (interviews) as well as any other possible form of contribution useful to the study such as technology impact references or even a joint session with the stakeholders involved in the study.

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