FastICpix: Integrated Signal Processing of Active Hybrid Single Photon Sensors with ps Time Resolution

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ABSTRACT

FastICPix is a novel reconfigurable low light-level hybrid detector concept that can be scaled to arbitrarily large areas and that aims to measure the position and the time of arrival of single photons with ~10 ps time resolution, bringing a revolution in medical imaging and other Time-of-Flight applications. FastICPix consists of an array of groups of SPADs 3D-connected to a pixelated readout ASIC based on novel reconfigurable architectures. In ATTRACT phase-I we have focused on developing these architectures and implementing fast front-end circuits and TDC banks in 65 nm CMOS technology. FastICpix concept has been validated by simulation.

Keywords: single photon sensor; ASIC; CMOS; SiPM; SPAD; ToF, PET, Mass Spectrometry, TOFMS, LIDAR, FLIM.

1. INTRODUCTION

The goal of FastICPix is to open the path to the ultimate large area, Low Light-Level (LLL) sensor. It is a pioneer for a new family of hybrid sensors in photonic science and technology. It introduces a new development methodology in which the signal processing is embedded in the sensor, a large area LLL integrated vision system which extracts timing information from incoming light with 10 ps precision even for a single photon. This project has a huge transformational impact on society, from medical and molecular imaging, to transport or homeland security. Specific application cases will be discussed in section 5.3.

Silicon Photomultipliers (SiPMs) are unrivalled low mass detectors for high time precision measurements in low light environments. Both analog and digital versions exist and each has its own limitations. In analog SiPMs, the outputs of multiple Single Photon Avalanche Diodes (SPADs) are connected together leading to a large capacitance, thereby limiting Single Photon Time Resolution (SPTR) and increasing the dead time of the readout channel. Digital SiPMs, on the other hand, have readout electronics associated with every SPAD, thus improving the SPTR, at the expense of Fill Factor and hence Photon Detection Efficiency (PDE). Moreover, for power consumption reasons it is difficult to incorporate one Time-to-Digital Converter (TDC) per SPAD on large area systems. We propose a novel hybrid solution that aims at achieving large detection areas with a time resolution determined by the intrinsic resolution of the SPAD. In this architecture, groups of SPADs (or SiPM pixels) are connected to a pixelated readout Application Specific Integrated Circuit (ASIC) using Through Silicon Vias (TSVs) and bump bonds. The pixel in the readout ASIC comprises an analog front-end (FE), a discriminator and a TDC. The proposed solution is programmable in order to optimize the system performance for different applications, by varying the pitch of the pixels and/or the use of signal summing in neighbouring pixels.

We have designed the key building blocks of the FastICPix CMOS chip and have proved the concept by means of a Full Monte Carlo simulation. We have studied, following both analytical and numerical approaches, different ASIC input stage configurations, considering sensor segmentation, interconnection parasitics and power consumption. We have identified an optimal configuration in which the electronics noise contribution can be well below 10 ps, with a power consumption lower than the one of existing SiPM readout systems. This has guided the design of the analog signal processing, TDC and Clock Distribution Network (CDN).

2. STATE OF THE ART

SiPMs are used for low light level sensing, but for large channel areas (>1 mm^2/ch) their time resolution reaches at best 100 ps[1] for analog implementations [1] and 200

[1] Full width at half maximum (FWHM) are used across the document unless explicitly stated otherwise.

ps [2] for digital implementations. Analog SiPMs offer the best performances in terms of PDE, Dark Count Rate (DCR) and optical crosstalk because they are fabricated in processes optimized for the detection of light. However, due to the parallel connection of many SPADs, they present two intrinsic limitations: (1) the large parasitic capacitance degrades the SPTR and (2) it is not possible to time stamp multiple photons closely spaced in time. On the other hand, Digital SiPMs do not present these limitations, but they require some active electronics per SPAD, which limits the Fill Factor (FF). An advanced 3D process (< 4 µm vias, <50 µm pitch) is required to improve the FF, which implies high development costs and potential initial yield issues, in particular when operating at low production volumes. Moreover, the requirement of a TDC per SPAD imposes a large power budget because the consumption for a 10 ps resolution TDC is much higher than 100 µW [3] and a SiPM for PET has typically a few thousand SPADs. In this case, the power consumption per SiPM would be well above 1 W (about 100 W per module).
A better compromise is the architecture of column MD-SiPM [4] (Multi Channel Digital SiPM), which shares a number of SPADs per TDC. However, this means that for MD-SiPMs a trade-off between the efficiency in detecting the photon time stamps and the power consumption exists.
In summary, neither large area analog nor digital SiPMs (of more than 1 mm^2), achieve a SPTR of below 100 ps. The aim of FastICpix is to achieve a SPTR ~20ps on large detection areas.

3. BREAKTHROUGH CHARACTER OF THE PROJECT

As shown in Fig. 1, FastICpix is a new sensor with adaptable segmentation that explores a huge space of solutions between analog SiPMs (no segmentation) and digital SiPMs (full segmentation). FastICPix is a hybrid solution using 3D interconnection techniques, optimized sensors and novel readout electronics techniques in order to explore the optimal segmentation.
A key characteristic of FastICPix is its reconfigurability: the segmentation factor optimized to the application. The pixels are configured so that the signals from different sensor elements can be summed, which also contributes towards a configurable granularity as small as ~300 µm pitch. It is possible to achieve a trade-off between time resolution, spatial resolution, power consumption and event data rate to optimize the operation of the hybrid sensor to different applications. FastICpix is a sensor concept based on the readout of groups of SPADs by a readout chip.
The SPADs are grouped in clusters and connected to the back-side of the sensor chip by means of a TSV process [5]. A Redistribution Layer (RDL) is also implemented to connect the TSV with the bump-bonding pad. The bonding pad is connected to a readout circuit designed in 65 nm CMOS technology. The intimate connection between sensor and readout electronics aims at reducing the parasitic interconnect components.

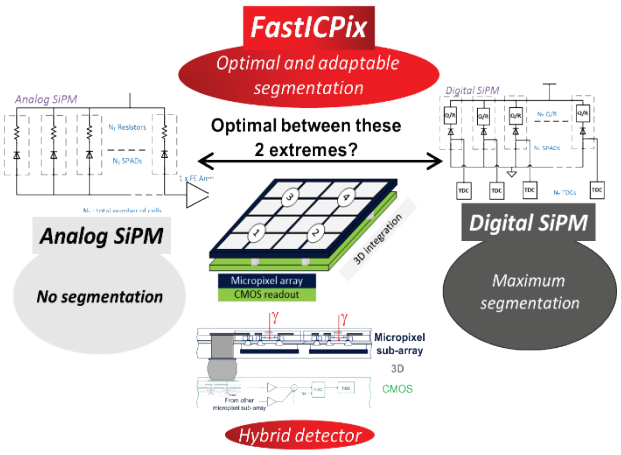

Fig. 1. FastICPix is a hybrid solution using 3D interconnection techniques, optimized sensors and novel readout electronics techniques in order to explore the optimal segmentation.

The dramatic reduction of the input capacitance achieved by segmentation results in a larger current signal at the input of the FE, which is crucial to reduce the jitter. FastICPix is designed with a novel layout architecture, such that the detector can be tiled seamlessly on 4 sides to build large detection areas.
In our initial studies, we focused on the readout of groups of SPADs; however, FastICPix is a platform that allows connection and readout of the signals of other sensors with intrinsic amplification, such as Micro-Channel Plates (MCPs).

4. PROJECT RESULTS

The FastICPix design concept has been studied using funding from this ATTRACT phase I grant. This section aims at summarizing the findings of this study.
We have investigated the choice of parameters to integrate the sensor with the FE. The range of input FE impedances to avoid oscillatory response has been calculated. Since the aim is to optimize the SPTR, i.e. the jitter for the signal of a single photon, the noise has to be minimized and the slew rate maximized (a system with a leading-edge discriminator is considered). There is also an optimum FE bandwidth, which should be high enough to preserve the slew rate of the signal at the output; and low enough to effectively filter noise at the output of the FE. The optimal segmentation of a SiPM has been calculated: two expressions have been obtained to identify the minimum number of SPADs below which (1) segmenting does not improve noise due to the dominance of the parallel noise, which does

not scale with the capacitance, and (2) the slew rate does not improve [7]. This is illustrated for a specific configuration in Fig. 2.

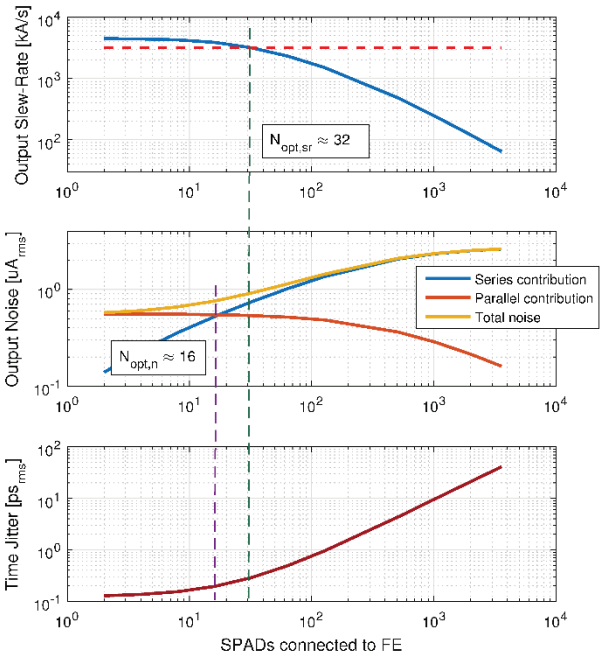

Fig. 2. Simulation of the slew-rate, preamplifier noise and time jitter for different number of SPADs connected to a single FE [7].

In order to time stamp the incoming photons, a TDC is implemented per pixel. The TDC, shown in Fig. 3, is based on a ~2 GHz (nominal) ring oscillator with 12 phases that is started with the arrival of a signal and is stopped at the following rising edge of the system clock (≤100 MHz). As a result, the oscillator is only working a small fraction of time, reducing power consumption.

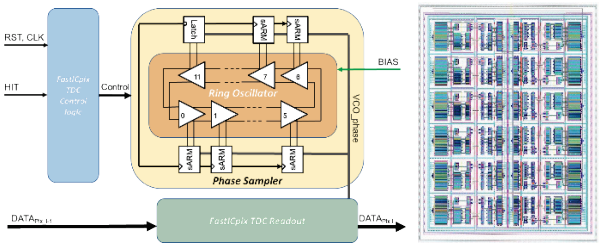

Fig. 3. TDC block diagram (left) and ring oscillator layout (right).

The power consumption related to the TDC bank of N_{TDC} units has a constant term per TDC and a term proportional to the hit rate (f_h expressed in MHz), for a 10 mm^2 sensor:

$$P_{TDC\_BANK} = 20 \cdot N_{TDC} + 150 \cdot f_h \ [\mu w]$$

The photon arrival time is interpolated in two steps: first, a counter increases its value with every oscillation of the ring, and second, the internal phases of the ring oscillator are latched at the rising edge of the system clock in order to obtain a fine time measurement (20 ps time bin).

A study on how to distribute a very low-jitter system clock to all the pixel elements with low power consumption is in progress. It is based on the Timepix4 Clock Distribution Network (CDN) architecture, which consists of digital Delay-Locked Loops (DLL). In the dDLLs, the delay line is distributed along two columns of pixels, and a phase comparator and a control system are located at the end of every double column [8]. The novelty in the approach for FastICpix is that the control of every delay cell in the Digitally-Controlled Delay Line (DCDL) is done individually, which provides a finer adjustment of the delay of the line and thus reduces the systematic error associated to the CDN. The CDN can be scaled to arbitrary chip areas as indicated in Tab. 1. Such a scalability is provided by changing the number of nodes in the DCDL, the master clock frequency and the number of dDLLs in the CDN. The expected total power consumption in each case is also indicated in the table, showcasing that the CDN is not the dominant contribution in the overall chip consumption.

Tab. 1. Guidelines to scale the CDN to arbitrary chip areas

Chip area (cm^2)	Number of pixels)	Number of DCDL stages	Master clock freq. (MHz)	Number of dDLLs	CDN power (mW)
0.3x0.3	8x8	8	80	2	0.6
0.6x0.6	16x16	16	75	4	1.6
1.2x1.2	32x32	32	40	8	6.1
1.8x1.8	48x48	24	50	24	13.9
2.4x2.4	64x64	32	40	32	24.2

The final optimization of the FastICpix configuration is based on previous studies. Optimal segmentation and FE design are studied, considering the power consumption per photo-sensor area. We have explored different configurations and segmentations, which involves the following parameters:

- N_{FE}: number of sensor segments and thus number of FE input stages.
- N_{TDC}: number of TDCs
- F_{SUM}: analog summation factor, $F_{SUM} = \frac{N_{FE}}{N_{TDC}}$.
- P_{TOTAL}: total power consumption, which is $P_{TOTAL} = P_{FE} + P_{SUM} + P_{TDC\_BANK} + P_{CDN}$

Fig. 4 illustrates the electronic noise contribution to jitter as a function of the aforementioned parameters, for common source (CS) and common gate (CG) configurations. A first conclusion is that both CS and CG configurations can achieve optimal time resolution for a large TDC bank, thus N_{TDC} matching N_{FE}. In practice, N_{TDC} will be limited to ≈10/mm^2 because of area constraints. Secondly, the CS configuration achieves picosecond jitter with a sensor segmentation factor (N_{FE}) > 16.

This result substantiates that FastICpix allows to exploit the intrinsic SPTR of SPAD (as low as 20 ps for

FBK's NUV-HD devices [1]) to build a large area sensor with such timing performance.

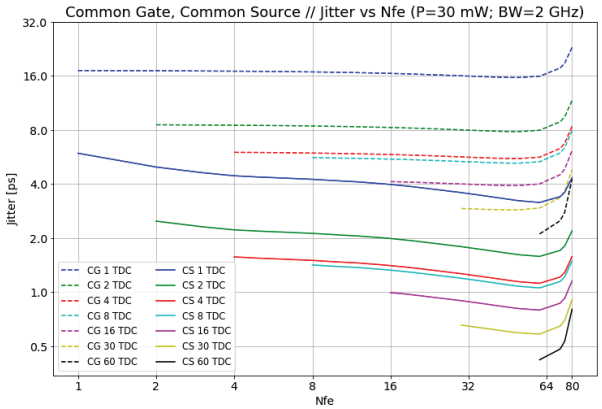

Fig. 4. Electronic noise contribution to jitter (rms) as function of N_{TDC} and N_{FE}, for CS with 500 Ω input impedance and CG configurations and for P_{TOTAL}=3 mW/mm^2. Total sensor area is about 10 mm^2 with 50 µm SPAD cells biased at 4.5 V over-voltage. P_{SUM}=0.33 mW·N_{FE}.

We have developed and validated a full Monte Carlo simulation framework [6], which includes physical simulation of the light generation and transport and electrical simulation of the sensor and the readout electronics. In order to illustrate the impact of our achievements, we have simulated a ToF-PET detector consisting on a 3x3x5 mm^3 scintillator with very high initial photon-time density (IPTD) readout by FastICpix. The scintillator has 30 ps rise time, 1.5 ns effective decay time and a light yield of 10 photons per keV. Even if a scintillator with such IPTD is not yet usable for PET application due to low efficiency, there are promising R&D efforts on this direction [9]. FastCIpix has is configured with N_{TDC}=N_{FE}=64 and the sensor layer is as described above and with a PDE of 60 %. According to our preliminary simulations, a CTR of 30 ps is achieved after averaging the 12 fastest TDC time stamps. It is worth to mention that the Monte-Carlo simulations naturally include effects like the 511 keV gamma depth of interaction (DOI). Part of our future work is to study DOI correction techniques.

5. FUTURE PROJECT VISION

5.1. Technology Scaling

The ATTRACT phase II will be dedicated to build a FastICpix prototype detector module and to demonstrate the concept in relevant applications. Once achieved phase II, the design will be in a Technology Readiness level 7 (TRL7) or higher and ready to be a commercial product. The sensor will be developed by Fondazione Bruno Kessler (FBK). The detector module will consist of a Backside-illuminated (BSI) SPAD layer with a FastICpix readout chip connected using 3D integration techniques. Back Side Illumination will improve performance dramatically, achieving a fill Factor close to 100% even for smaller cells and hence reducing the correlated noise (which also affects timing). In any case, Front Side Illumination will be maintained as back-up option for near-UV sensors.
The 3D integration enables to optimize the time resolution of the system and also allows tiling detector modules seamlessly on 4 sides. The hybrid concept allows optimizing SiPM sensor layers to very different applications as the ones mentioned in the next section.

5.2. Project Synergies and Outreach

FastICpix has synergies with several phase-I projects. Photoquant project which aims at exploiting nano-photonics for developing a new generation of highly efficient and ultrafast single-photon quantum sensors. A combination of Photoquant sensors and FastICpix readout electronics developments will be straightforward and with high impact.
There are also synergies with phase-I projects focused on specific applications, such as Posics. FastICpix offers a power optimized readout and the feature of programmable granularity.
Academic dissemination (conferences, journals, etc) will be based on the EC open access policy. We also plan to organize multidisciplinary workshops on photo detection technology and applications, and webinars and bootcamps to present the product to the industrial and scientific audience.
Communication will be conducted in synergy with the EC to enforce its impact and benefit from the existing knowledge and infrastructure in the EC community (news, events, magazine). The website will have a part for general public with a presentation of the project and participants, multimedia material, press releases and interviews with PIs of the project. As an example, we count on an official website [10] and a general public video [11], thanks to the collaboration with the Technology for Social Impact (TeSI) students' team.

5.3. Technology application and demonstration cases

FastICpix can have a Transformational Impact in a wide range of applications: in medical imaging, as said above, 10 ps PET can be demonstrated in collaboration with R&D projects on prompt light production mechanisms. This opens the door to a 10-fold increase in sensitivity: reduction of radiation dose, scan time, and cost by an order of magnitude.
In Time of Flight Mass Spectrometry (TOFMS), the introduction of FastICpix allows: 1. miniaturization; 2. an increase in the data throughput; and 3. an improvement in the sensitivity of the measurement because ions can be discriminated individually. In the medical field, this paves the way to: (1) the capability to image thousands of molecules in a single experiment without labelling; (2) minimal sample pre-treatment; (3) improvements in signal-to-noise ratio and mass sensitivity; (4) reduction in the time required to obtain

results; and (5) portable point-of-care applications and personalized treatments.

In Fluorescence Lifetime Imaging (FLIM), this project can have a large impact for the domain of low illumination applications, such as lightsheet fluorescence microscopy or total Internal Reflection microscopy. A great advantage of combining FLIM with lightsheet microscopy is that it enables functional imaging having applications in immuno-oncology, immunology, and neuroscience among others.

In quantum communications based on entanglement, high rate and timing resolution is a key factor. FastICpix can help to improve gating techniques.

Finally, high luminosity particle colliders require picosecond timing with single or few photons. Typical use cases are RICH or timing layers. The FastICpix team has already joined efforts with groups in LHCb (RICH and TORCH) and Belle II RICH.

5.4. Technology commercialization

The transfer to industry can be smooth for several reasons. First, the ASIC technology is based on a commercial standard CMOS technology, which can be manufactured in large scales. The novel circuit techniques to achieve the 10 ps time resolution have been validated in the Phase I. Second, the sensor technology will be developed using standard Silicon Wafer processing techniques with partners that have solid experience in technology transfer. And finally, the 3D integration technology of more than 100 µm TSV pitch required is already available.

Furthermore, an advisory board (AB) is foreseen, inviting experts from industry in different application areas. Confidential discussions are ongoing with different sectors, from photosensor technology to medical imaging, mass spectrometry, LIDAR, Quantum technologies and FLIM.

Two non-exclusive strategies to market are considered. In a first approach, FastICpix is developed for selected applications, which showcases the value of FastICpix to the target industry and attract stakeholders in specific fields. In a second approach, FastICpix is presented as a standalone product for multiple applications.

5.5. Envisioned risks

The main challenge of phase-II is the requirement of the best SiPM/SPAD technology. This is ensured by the participation of a leading institution in the field of SiPM technology (FBK). Two development lines are pursued to ensure the completion of at least one successful photodetector: a conservative line, based on a mature FSI technology with 0.5 mm TSV pitch; and a higher risk/higher benefit line, with BSI, 0.3 mm TSV pitch and thinned glass for enhanced NUV detection.

5.6. Liaison with Student Teams and Socio-Economic Study

The FastICpix team has collaborated with a TeSI student team in phase-I. The experience has been excellent and enriching, producing relevant inputs at different levels. First, new applications, such as TOFMS or FLIM, have been identified thanks to this collaboration. The TeSI team has enabled the contact between the FastICpix and application experts. Secondly, a video to communicate the FastICpix concept and applications to the general public has been produced [11]. And finally, the team has proposed strategies to the market.

For phase-II, we plan to improve the training of MSc in order to provide a solid understanding of the technology to the team of students, and to make this transfer faster. A senior member of the team will prepare such a training in collaboration with PhD students involved in the project, as well as providing information to the expert-driven socio-economic study of ATTRACT.

6. ACKNOWLEDGEMENT

"This project has received funding from the ATTRACT project funded by the EC under Grant Agreement 777222"

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