LIROC : Novative RadHard Front-End ASIC for Lidar

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ABSTRACT
LIDAR is a distance and speed measurement device using reflection characteristics of emitted light. Space industry is using LIDAR to scan planet surfaces before landing missions, to measure distances between spacecraft and for many other applications. Having the most sensitive detector is critical to measure long distances, particularly in space applications. First LIDAR-dedicated silicon photomultipliers are getting on the market among other detectors such as photomultiplier tubes. However, no dedicated electronics is available so far. Main read-out requirement of LIDAR read-out is an excellent timing resolution and a 2ns double-peak separation. None of the ASICs on the market allows such a fast response. Our consortium has designed a LIDAR dedicated multi-channel read-out chip prototype focusing our R&D on bandwidth and fast return to baseline to fulfil LIDAR requirements.

Keywords: Microelectronics; Front-end; ASIC; LIDAR; SIPM; PMT; Radhard.

1. INTRODUCTION

Microelectronics team in labs and in industry has been designing front-end electronics for photodetector read-out for decades. Most commonly optimized parameters are:

- Dynamic range;
- Energy resolution (charge resolution);
- Time resolution;
- Event rate

Requirement specifications for existing ASICs have been provided by scientific instrumentation and medical imaging needs in which both integrated energy and time of arrival are needed to reconstruct events. Few projects are using photon counting to reconstruct energy instead of regular analog integration [1].
LIDAR read-out requires a fast photon counting over 100MHz and a 2ns double-peak separation thus a capability of measuring distinctly two consecutive 2 ns-separated photons [2].
None of the integrated electronics available in the scientific community reaches such specification. LIROC consortium has designed a LIROC ASIC which is a radhard 64-channel fast front-end ASIC dedicated for LIDAR application and fulfilling all its requirement specifications.

2. STATE OF THE ART

Many SIPM (Silicon Photomultiplier) read-out ASIC have been designed since creation of that novel photodetector in the early 2000's. Some of these ASIC are presented in Table 1.

Table 1 - Some existing SiPM read-out ASIC

ASIC name	Manufact.	ch	Information
SIPHRA[3]	IDEAS	16	SIPHRA is designed for spectroscopy application and does not have the required timing resolution
NINO[4]	CERN	8	NINO has excellent timing performance for time of arrival. However this ASIC is measuring energy using time-over-threshold features and return-to-baseline is not compatible with LIDAR application for pulse separation.
PETA5[5]	HEIDELBERG UNIVERSITY	64	PETA5 ASIC is specifically designed for PET application and cannot trig on double pulsed light as required by LIDAR application
TOFPET2[6]	PETSYS	64	TOFPET2 ASIC is specifically designed for PET application and cannot trig on double pulsed light as required by LIDAR application
PETIROC2A [7]	WEEROC	32	PETIROC2A ASIC is specifically designed for PET application and cannot trig on double pulsed light as required by LIDAR application

These ASIC have shown excellent performances for the application they were designed for but none of them can handle the 2ns required double-peak separation for a LIDAR application.

3. LIROC ARCHITECTURE

LIROC ASIC is designed in TSMC 130nm CM013G. This technology has been qualified by CERN for its excellent radiation hardness over total irradiation dose. Block scheme of LIROC is shown in Figure 1.

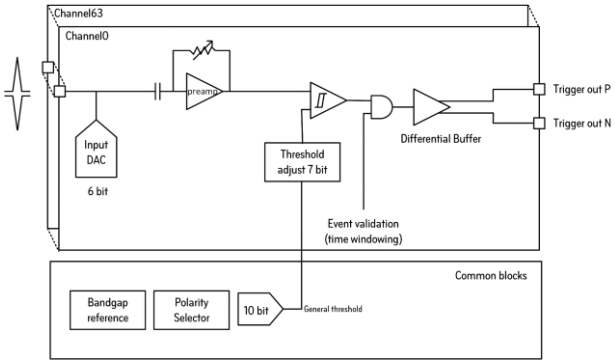

Figure 1 - LIROC block scheme

LIROC is a 64-channel front-end ASIC designed to readout silicon photo-multipliers (SiPM) for LIDAR application.
LIROC allows triggering down to 1/3 p.e. and provides low-voltage differential trigger output for each channel with an excellent timing resolution (better than 20ps FWHM) and excellent double-peak separation (100% efficiency on 5ns separated single photo-electrons). LIROC allows fast single photon counting over 100MHz per channel.
An adjustment of the SiPM high-voltage (gain) is possible using a channel-by-channel 6-bit DAC connected to the ASIC inputs. Channel-by-channel calibration on the trigger threshold is also possible thanks to 7-bit DACs. LIROC can be calibrated using the dark noise of the SiPM.
LIROC features a GHz measurement line composed of an RF preamplifier with pole zero cancellation followed by a fast discriminator and low swing LVDS fast driver. LIROC simulated performances and main features are presented in Table 2.

Table 2 - LIROC main features and performances

Detector Read-Out	SiPM, SiPM array
Number of Channels	64
Signal Polarity	Positive or Negative (selectable ASIC-wise)
Sensitivity	Trigger on 1/3 of photo-electron
Timing Resolution	Better than 20 ps FWHM on single photo-electron Better than 5ns double-peak separation on single photo-electron
Dynamic Range	Over 100MHz photon counting rate
Packaging & Dimension	BGA 20x20 mm2 Flip-Chip low inductance packaging technology
Power Consumption	210mW (TBC) – Supply voltage : 1.2 V
Inputs	64 analogue inputs with independent SiPM HV adjustments
Outputs	64 LVDS triggers
Internal Programmable Features (I2C)	64 HV adjustment for SiPM (64 x 6 bit), trigger threshold programming (10bits), 64 x 7 bit channel-wise threshold adjustment, ASIC-wise polarity selector, preamp gain adjustment, individual trigger masking and cell powering.

4. LIROC SIMULATION & LAYOUT

Recent sanitary crisis has delayed fabrication of LIROC ASIC. First results are expected in October 2020 instead of March 2020. Simulation results are presented in this section and silicon measurement results will be published when available.

1.1 Preamplifier AC simulations

Input impedance of preamplifier has been simulated at 60 Ohms and is stable across PVT (Process Voltage Temperature) corners (Figure 2). Input impedance is an important parameter to consider to avoid impedance rupture and bad transmission of photodetector signal at high frequency.

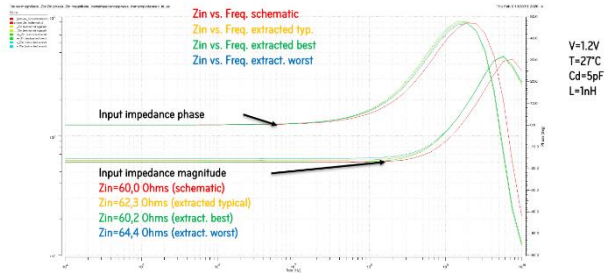

Figure 2 - LIROC impedance versus frequency (simulation)

Preamplifier bandwidth has been simulated above 1.4GHz with parasitic extracts (Figure 3)

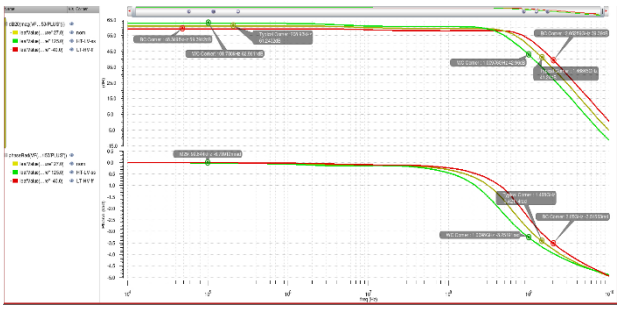

Figure 3 - LIROC bode diagram (simulation)

1.2 Full Chain Transient Measurement

Transient simulation has shown a quick return to baseline and in specification double peak separation on all PVT corners with parasitics extract. Typ. (typical) BC (best case) and WC (worst case) model parameters have been simulated with WC and BC parasitic extraction.

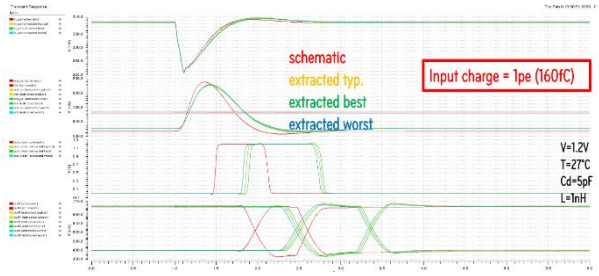

Figure 4 - Transient simulation for whole channel

Simulations shown in Figure 4 and Table 3 validate 2ns double-peak separation capability in most cases. That double peak separation can only be achieved with minimum signal of 1pe to keep the trigger width below 2ns.

Table 3 - LIROC simulated performances synthesis

Corner	Typ.	Typ& WC parasitic	BC & WC parasitic	WC & WC parasitic
Pre-amp output @1p.e	271.7 mV	240.6 mV	205.2 mV	147.2 mV
Pre-amp time occupancy @1p.e	1.8 ns	2 ns	1.63 ns	2.75 ns
Discriminator Width @1p.e Threshold	628 ps	827 ps	679 ps	1.2 ns
Pre-amp Bandwidth	4 GHz	1.5 GHz	2.1 GHz	1 GHz
Pre-amp transimpedance	61 dB	61 dB	59 dB	62dB
Pre-amp input impedance	60 Ohm	64 Ohm	44 Ohm	100 Ohm
RMS noise	1.1 mV RMS	1 mV RMS	1 mV RMS	1 mV RMS

1.3 LIROC Layout and packaging

LIROC has been layouted using a bump bonding technology to reduce parasitic inductance due to packaging interconnect. ASIC has a size of 11.2mm*4.8mm and has a total of 513 bump pad as shown in **Figure 5**.
ASIC is packaged in a custom FCBGA (Flip Chip Ball Grid Array) with 23 rows and columns of balls at a 0.8mm pitch to accommodate aerospace standard (**Figure 6**. Quality level insurance and associated package will be addressed after validation on a bread board. A custom substrate has been designed (**Figure 7**) using RF techniques to minimize parasitic and keep ASIC bandwidth beyond 1 GHz.

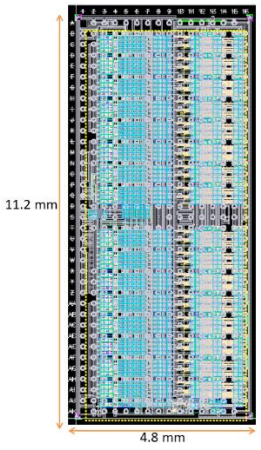

Figure 5 - LIROC silicon layout

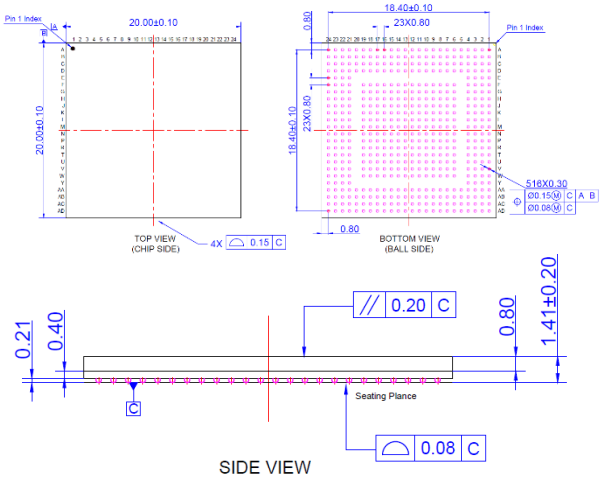

Figure 6 - LIROC FCBGA package mechanics

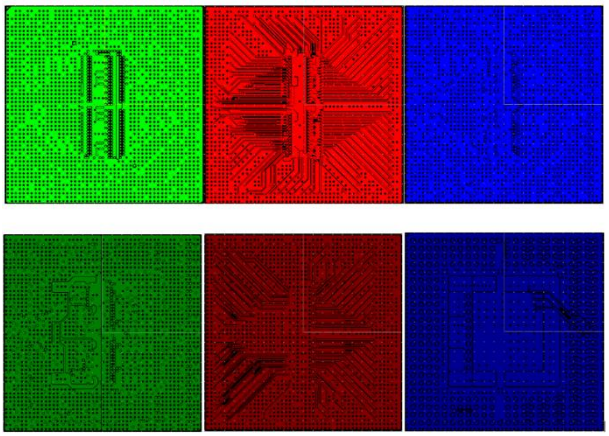

Figure 7 - LIROC custom package substrate layout

5. FUTURE PROJECT VISION

LIROC has raised interest of several actors in the photodetection and aerospace domain. Active NDA forbid our consortium to disclose current partnership or commercial discussion nevertheless the following information can be provided:

- Discussions with a SiPM manufacturer are ongoing regarding assembly of a LIDAR receptor module based on SiPM.
- Discussions with a PM tube manufacturer are ongoing regarding assembly of a photodetector module using LIROC for fast photon counting.
- Discussions are ongoing with a company designing 3D cameras to design a cost-effective LIDAR system based on LIROC technology.
- LIROC has been selected as a prime candidate to fly on an upcoming scientific mission on a Jupiter satellite. Work is ongoing to build a LIDAR using that technology. This project is the first LIROC customer. A first LIDAR product can arise from that first mission.

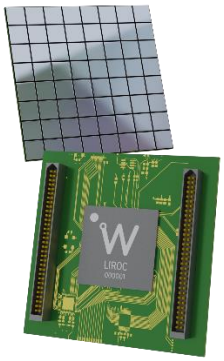

Figure 8 - LIROC LIDAR receptor product (artist view)

5.1. Technology Scaling

Technology scaling to TRL8 will be conducted in collaboration with first LIROC customer. Beyond the first mission on Jupiter satellite, several missions in aerospace industry has shown interest in such a LIDAR.
A collaboration with the LIDAR manufacturing will be set up apart the current mission and a product will be designed.
Aside aerospace industry, photodetector manufacturers have shown interest and product based on LIROC and their photodetectors will be designed upon first project success.
An industrial version of LIROC aiming cost-effectiveness and high volume is envisioned and shall be discussed after high-end project success.

5.2. Project Synergies and Outreach

Several synergies have emerged from ATTRACT meeting.
RANDOM POWER project is seeking for a read-out electronics for true random number generation and a synergy with LIROC consortium has been created.
WPET is looking for a compact and low power electronics for its wearable PET and LIROC performances and low power could be used to read-out that detector.
Public dissemination of LIROC project will be ensured by first product that will equip a lander to a Jupiter satellite. If mission will not be launched before the end of ATTRACT phase 2, instrument choice will be done by then and communication will be based on that first success.

5.3. Technology application and demonstration cases

ATTRACT phase 2 would allow LIROC consortium to expand and include photodetector manufacturers and LIDAR manufacturers to build an end-to-end collaboration that could build an industrial product based on aerospace product. Ground application of such LIDAR are numerous and can disrupt these domains:

- *Automated logistics;*
- *Robotics;*
- *Automated and autonomous transportation;*
- *Smart city and smart building.*

5.4. Technology commercialization

Weeroc has already a worldwide distribution network through its partnerships and LIROC would be commercialized using that existing network.

5.5. Envisioned risks

Interest and market in the aerospace industry have already been demonstrated for LIROC. Scale-up from Hi-Rel aerospace standard to SIL industry standard is the most difficult part of the project evolution.
Consortium is already in contact with an industry SIL standard specialist that would be part of the consortium for that matter.

5.6. Liaison with Student Teams and Socio-Economic Study

A dedicated strategic marketing action will be engaged in parallel of industrialization of LIROC. The aim of that marketing action is to:

- Find possible market not detected in first study;
- Sense market and tune the product to fit needs;
- Estimate volume and target cost to validate feasibility and profitability.

Connection with student team will be done through existing marketing and distribution team.

6. ACKNOWLEDGEMENT

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