Mini CdTe on Chip – MC2

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ABSTRACT
Assembly of heterogeneous ASICs in electronic devices enables innovative functions in miniature systems in the field of detection and imaging for Space Science, Synchrotron radiation measurements, Medical imaging and more. High density electronics is a trend in hard X-ray (HXR). We unlock a disruptive technology for high-density and large-scale manufacturing of CdTe HXR imaging-spectrometers, based on 3D epoxy packaging to stack functions without Through-Silicon-Via. It relies on a wafer-level process to build high performance 3D detection modules made of circuits from any ASIC foundry, including Multi Projects Wafers, often the sole reasonable economic way for labs to access deep submicron nodes.

Keywords: full custom ASICs; 3D Stacking; WDoD™ ; CdTe, Hard X-rays ; Imaging Spectrometers.

1. INTRODUCTION

Assembly of heterogeneous integrated circuits in high-reliability 3D components allows to create innovative functions in miniature systems in the field of detection and imaging. Whatever the field of application (Space Science, Synchrotron detectors applied to XRF, Medical imaging, 3D printing monitoring, ...), the density of electronics is growing up as embedded systems are increasingly sophisticated to offer progressively highly autonomous functions. This is a trend for imaging spectrometers in the hard X-ray range (HXR) as well, the target of the MC2 (*Mini CdTe on Chip*) ATTRACT project.

The goal of MC2 is to explore a disruptive 3D integration technology to create a large surface (~4 cm^2), fine-pitch (~250 µm) and high energy resolution CdTe imaging spectrometers read out by a mosaic of smaller (~1 cm^2) affordable deep sub-micron ASICs from Multi Project Wafers.

The breakthrough relies on a technology for high density, large scale, highly reliable manufacturing of CdTe imaging spectrometer based on a wafer-level epoxy packaging by compression molding technique to stack electronic functions in 3D without any Through-Silicon-Vias.

We completed an exploratory study to evaluate the feasibility of such an integration technology building prototypes of the front layer of a detector module. A compression molding panel comprises a mosaic of advanced full custom ASIC, previously designed at CEA. D2R2 (a new release of the D2R1 [1]) is a low noise 2D ASIC able to readout 1024 independent CdTe 250µm pitch pixels. Bringing 4 chips side by side with the strong requirement of limiting inter chip dead zones is delicate. Moreover, the outer pad ring comprises more than a 130 I/O's along two sides of the ~8.5x8.5 mm^2 circuits, challenging the technology for integration and routing in a unique redistribution layer (RDL). The chips have been specifically prepared for integration. The compression molding process has been implemented with state-of-the-art epoxy resins with very fine silica filler. Prototype mosaic panels have been successfully realized and satisfactory position accuracy has been obtained to guarantee a regular pixel alignment from one circuit to another as well as a dense I/O ring. For that purpose, we developed a custom optimized layout router to draw the necessary RDL and automatically creates the detector pixel pattern to complete a monolithic crystal flip-chip on top the ASIC array. A panel demonstrator with a mosaic of circuits will be produced shortly.

2. STATE OF THE ART

Pixelated CdTe spectrometers are promoted in different groups with different philosophies:

Double sided strip CdTe [2] are based on cross-strip configuration, reading a large number of virtual pixels (128x128) with a limited number of readout channels (256). The resolution is 1.3 keV FWHM at 60 keV over

a 64 mm^2 area. The performance degrades for larger areas [3]. The cross-strip configuration is not buttable.
A 250 µm pitch CdTe array with 80x80 pixels has been developed at RAL [4]. An energy resolution of 760 eV FWHM at 60 keV is obtained. The frame readout mode is a limitation for high counting rates. This configuration can be tiled thanks to TSV [5]. Large ASIC reticules are used. Further development in deep submicron technologies would be financial show-stoppers for scientific labs.

In the current state of the art, it is extremely challenging to combine simultaneously large-scale fabrication of modular and buttable devices and performance in terms of energy resolution and pixel pitch. Moreover, stacking electronics and combining functions in 3D is essentially not approached for hard X-ray imaging spectrometers so far, except in our group [6, 7].

Prior to MC2 project, we have been developing at CEA a prototype made of a 16x16 pixels, 300 µm pitch [1]. We demonstrated a resolution of 584 eV FWHM at 60 keV. The current project is encouraged by this high performance which shows the readiness to push a disruptive approach in integration without TSV toward large detectors with fine pitch.

With regard to WDoD™ compression molding technology, 3D PLUS has produced 3D demonstrators and prototypes for different markets (miniature pacemaker [8], FPGA modules and Quad-Die DDR3 modules [9]). So far, WDoD™ has never been used for such demanding applications where large scale and detector performance are required.

3. BREAKTHROUGH CHARACTER OF THE PROJECT

Our technology will surpass the limitations of the current state-of-the-art combining photon counting, high energy resolution, fine-pitch and large detection area buttable on 4 sides in a wafer level fabrication process, bringing to the community an ultimate CdTe imaging spectrometers for science and applications. In addition, our project reinforces the feasibility of a wafer-level 3D integration process of large-scale applications or collective fabrication of a multitude of devices simultaneously. It can be applied in many fields of industrial applications (smart sensors, internet of things, advanced imaging technologies ...).
The principle relies on the construction of a mosaic of front-end ASICs embedded into a polymer matrix to form a flat and large plane of circuits whereon the pixelated detector is flip chipped. A single crystal is then read out by four independent circuits. The obtained microelectronics layer is processed with a wire free technology to bring the necessary interconnections (I/O's) at the back side using a laser grooving process. Thus, it can be stacked and interconnected to further circuitry such as power supply filters, thermo-mechanical carriers and analogue-to-digital converter stages for instance. The module is finished with an interconnection layer. The front-end circuits are based on a 2x2 ASIC array, forming a large surface 4 times larger than the unit circuit size. As a reticule is approximately 2x2 cm^2, a large crystal covering approximately 4x4 cm^2 can be envisioned without any Through-Silicon-Vias (TSV) at ASIC level. Minimizing the surrounding I/O pad ring surface, larger mosaic can be engineered with limited dead zones.

The breakthrough relies on the use of a wafer-level process to build a 3D detection module package offering both high performance and low dead zones in the sensitive area. This technology also allows the use of chips extracted from Multi Projects Wafers, an economic way for the labs to access deep submicron technologies, enabling the use of state-of-the-art technologies when large area applications are required such as pixelated detector arrays.

On the long run, commercially available deep submicron technology, down to 28 nm or less will be used for the design of ultra-fine pitch HXR imaging spectrometers.

4. PROJECT RESULTS

The functionality and basic performance measurements of our readout ASIC D2R2 have been performed before its integration into a technological demonstrator. Even though the final technological demonstrator of MC2 is not functional intentionally, we used real parts toward the design of a full functional detector in case of success. Moreover, the chip having 1024 pixels and 135 I/Os (109 used), D2R2 represents a challenge both in terms of electrical design, compression molding process and RDL routing. This is the core challenge of MC2.

The D2R2 chip has been successfully tested. All 1024 channels are behaving satisfactorily. We achieved 75 el. rms noise in average (Fig. 1) which corresponds to an average expected energy resolution of ~900 eV at 60 keV, good enough for the demo.

Because a monolithic CdTe detector must ultimately cover the mosaic of 4 ASICs, a precise and accurate alignment is required down to 15µm or less. For that reason, the chips have been carefully prepared and characterized (precise dicing and thinning) prior integration into a panel. Working on real dies makes sense from that prospective too. This is important not only for the pixel alignment of a CdTe detector flip-chipped on top, but also for the RDL over small I/O pads with a typical pitch of 90µm.

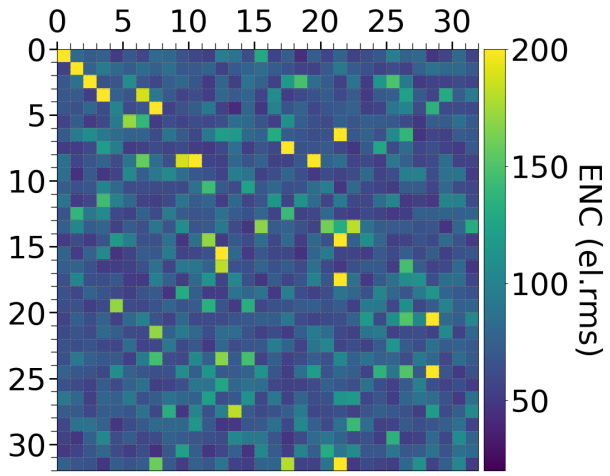

Fig. 1. Measurement of a noise map of a single D2R2 circuit, with 1024 pixels. The circuit is fully functional and noise is found to be 75 ± 21 el rms. (a diagonal of 4 shinny channels in the upper left corners are wire bonded to capacitive lines of a PCB for test purpose).

Finally, four adjacent circuits are placed as close as possible to each other. A space between two circuits is inevitable because the epoxy resin has to fill the gap and create a robust and cohesive assembly. Different gap sizes have been investigated. We successfully built a panel with a 132 µm gap after a careful selection of epoxy resin loaded with tiny diameter silica filler. 132 µm gap is the minimal value to simultaneously keep a cohesive structure and a regular pixel pitch from one quadrant to another. A smaller gap is achievable relaxing the constraint on pixel pitch regularity and/or reworking the pixel design, for instance moving the pixel pad to a different location closer to the edges.

Fig. 2 shows a mosaic we made. The sample consists of four D2R2 circuits (250µm pitch, 4096 pixels in total) in a compression molding panel, separated by ~132 µm inter-ASIC gap. 436 I/O's for power and control of the ASICs are distributed along the outer ring of the mosaic. An RDL will be deposited on top. In the end, the mosaic behaves like a virtual full custom circuit of 17x17 mm^2 by side. Interestingly, designing a full reticule size chip (~20 mm by side), a detector surface of 4x4 cm^2 is achievable with the same technology. The position of the circuits is guaranteed within 15µm accuracy during the compression molding process to allow both the RDL to be deposited on the I/O pads and a monolithic CdTe crystal to be flip-chipped on top of the 4096 pixels pads. The cross at the centre forces the inner central pixels to be larger than the others, with a local pixel size of 500 µm instead of 250 µm. The crystal being monolithic, this area is not a dead zone at the expense of a complex pixel pattern at detector level.

Another important challenge relies in the capability to route a single layer RDL with such a high number of lines. The tracks have to be routed to the side of a future 3D module and further away to a test socket. Naturally, changing the chip position parameters instantly affects the RDL routing as well as the detector pixel pattern. For optimization and design efficacy, we developed a full custom RDL router that takes all these constraints into account. The algorithm automatically creates the optimal routing for RDL, module, test socket and pixel pattern in one shot. Fig. 3 illustrates the result with a close-up view in a corner of the RDL layout. The pixel pattern is generated simultaneously with the tracks from the chip to the edge of a 3D module. The distance between the ASIC edges and the module edges is a dead zone. However, it is important to notice that this area is covered by the necessary guard ring surrounding the pixels at detector level.

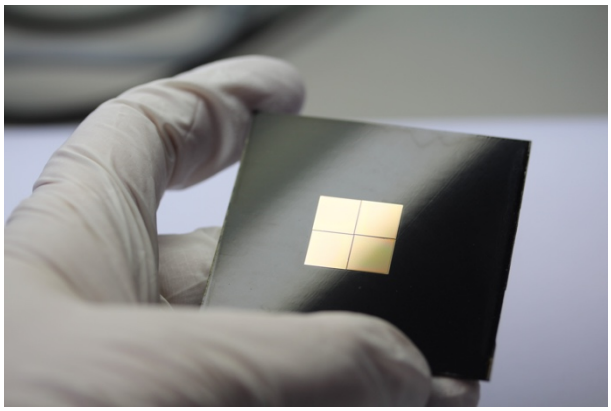

Fig. 2. Example of a 17mm by side mosaic realized in the frame of ATTRACT. The sample consists of four D2R2 ASICs in a compression molding panel.

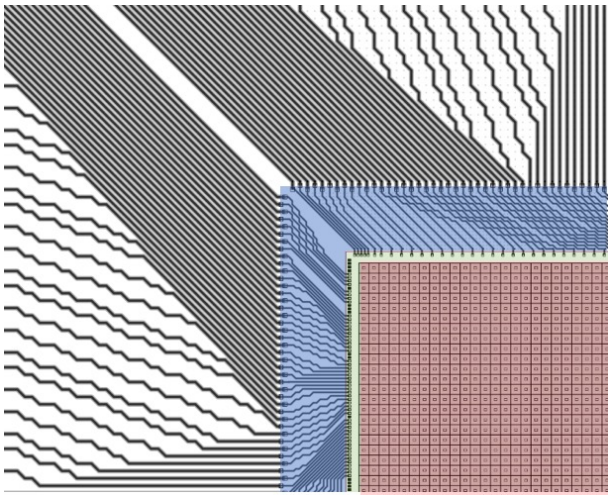

Fig. 3. Close-up view of the RDL: (Pink, bottom right corner) Pixel pattern design – (Green region) Outer ring pad of the chips – (Blue region) The fine tracks of the RDL are routed to reach the edges of a 3D module. Tracks here will be routed to an electrical circuit beneath without any TSV by means of 3D PLUS stacking and laser grooving process. This dead zone area is facing the necessary detector guard ring – (White region) Wider lines are distributed further to allow circuit testing before stacking above another circuitry to form a final 4-side buttable 3D detector module.

5. FUTURE PROJECT VISION

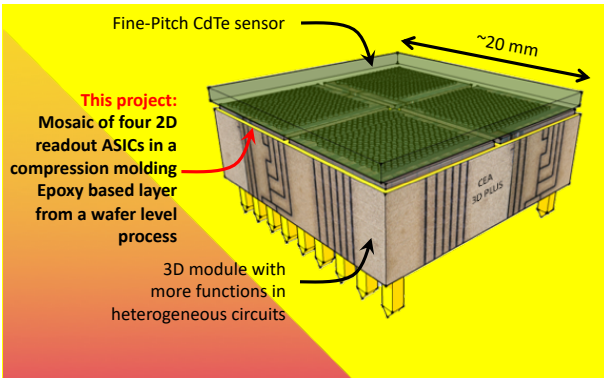

Fig. 4. For illustration, sketch of a complete 3D module wherein the front layer is made of the compression molding panel developed in the MC2 ATTRACT project.

The ultimate goal of MC2 is to produce a 3D modular detector unit including a front layer made of ASIC mosaic (ATTRACT phase 1) to readout fine pitch CdTe detectors flip-chipped on top a layer underneath to incorporate an analogue to digital converters (full custom ASIC in a different microelectronics technology), power supply filters, thermal drain for easy cooling and electrical interface. The 3D module will be buttable on its four sides so that large detector surface with high energy resolution can be created tiling detector modules on demand. The ASIC stacks and electrical services are molded according to 3D PLUS WDoD™ process to create the parts as thin as possible. The detector will look like the one sketched in Fig. 4.

5.1. Technology Scaling

ATTRACT phase 1 allowed to demonstrate the feasibility of the MC2 concept of a dense front-end electronics layer by means of a wafer-level compression molding technology. The technology concept has been formulated and initial proof of concept of one of the most delicate building blocks of the detector module has been proven so that we claim a TRL 2~3.

MC2 is coordinated by CEA (Research and Technology organization) and our industrial partner 3D PLUS (Company). By nature, the devices are realized using industrial means and platforms. MC2 is designed for easy scale up, for collective large panels, large reticule size full custom ASICs, maximizing the credibility of a detector module production for a variety of high-performance applications. Note that, the module has the potential to be space-qualified according to both CEA and 3D PLUS experience in the field.

Going forward requires an ambitious development to demonstrate a complete 3D module. This will bring the technology at TRL 5 with full functional prototypes in 3 years.

The main steps to scale-up are related to the D2R2 ASIC optimization (new release with simplified I/Os), design of a compete detector system, including electrical design, behavioural model, thermo-mechanical simulations, specific detector flip-chip process and testing (benches and firmware's developments). We emphasize the specificity of the flip-chip step which is peculiar in this domain. Indeed, CdTe flip-chip conditions are delicate and require low stress and low temperature process. In addition, the flip-chip on top of a few-mm thick 3D epoxy package is unusual.

5.2. Project Synergies and Outreach

To reach the ATTRACT phase 2 goal of a complete 3D detector module, the reinforcement of the consortium is desirable. Three new partners from academic and industry in Europe could join the group to reach TRL5 bringing specific competences in the fields of RDL (France), CdTe flip-chip (Germany) and device simulation and possibly for system electronics (Germany). With regard to concrete applications, two more partners are envisioned in the domain of space science for Solar Physics (US) and for Physics (Italy). The consortium is not yet fully consolidated. None of the five envisioned partners are involved in ATTRACT yet. With new partners, the budget for the phase 2 is estimated to be in the range of 1.5~2M€.

Because MC2 started at TRL1 and due to Covid19 crisis, public dissemination in phase 1 was refrained. However, dissemination of the work in phase 2 will rely on scientific publication in peer reviewed journals and each group will attend international conferences on an annual basis in the fields of X-ray detectors, microelectronics and 3D packaging.

5.3. Technology application and demonstration cases

MC2 is a cross-cutting project of component manufacturing, micro technologies, detector science and electronics. Application are in the field of fundamental physics (X-ray or charged particle detection system for research in physics and astronomy), medical applications (eg. theragnostic systems for radiotherapy) and radiation monitoring. This technology can be applied to many sectors where high energy photon counting sensor arrays have to be implemented. Moreover, MC2 will demonstrate an advanced wafer-level 3D integration process where collective fabrication of a multitude of devices simultaneously is needed.

In the frame of ATTRACT phase 2, two main applications are envisioned at first glance: A miniature HXR detectors is mandatory for space observation of the Sun for Space Weather. Focal planes for nanosatellite applications is an attractive outreach. Contacts with NASA are already in place. A second domain of application is the high-performance radiation monitoring in theragnostic systems to monitor the radiation dose in

radiotherapy, specifically in breast cancer. Contacts with French labs for experimental oncology are in place within CEA.

Finally, X-ray imaging spectrometers are of primary importance in synchrotron facilities. MC2 definitely can bring advantageous instrumentation at ESRF or at SOLEIL. Contacts with both facilities are foreseen.

5.4. Technology commercialization

MC2 module is finally a part that could be manufactured and commercialized directly. On the other hand, MC2, as a demonstrator, paves the way of high density WDoD™ technology for full custom parts by 3D PLUS.

5.5. Envisioned risks

The main risk for MC2 is related to the complexity of the device and success criteria based on high performance. The risk is mitigated by careful characterization and test of the components all along the integration process and rigorous product assurance and quality management. The project will be marked by reviews and milestones.

5.6. Liaison with Student Teams and Socio-Economic Study

Training through technological research and transmission of knowledge to students will be at the heart of the project. This aspect motivates the extension of the consortium towards academic institutions as anticipated, in the fields of microelectronics, process engineering, microfabrication and physics. At least, two PhD students will be recruited for long lead developments (ASIC design and physics applications) while MSc. Level students will be recruited for shorter studies along the development in all teams.

MC2 will be an active member of the ATTRACT phase 2 community responding to solicitation of experts by means of interviews and grand-public seminars.

6. ACKNOWLEDGEMENT

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