

# Near-infrared resonant cavity enhanced graphene/silicon photodetectors (REVEAL)

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## ABSTRACT

In this work a new concept of silicon-based resonant cavity enhanced photodetector operating at 1550nm has been proposed, designed, fabricated and experimentally characterized. Numerical simulations show as the resonant structure is able to increase the optical graphene absorption up to its theoretical limit of 100% at 1550nm leading to performance very promising for the mass production of low-cost near-infrared silicon photodetectors. Some prototypes have been fabricated and experimentally characterized. Ongoing work is focused on aligning the experimental results with the theoretical predictions. Finally, a future vision on this research activity has been accurately traced.

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*Keywords: Photodetector; near-infrared; silicon; graphene; Fabry-Pérot resonant cavity.*

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## 1. INTRODUCTION

Silicon (Si) photonics is nowadays an emerging market promising to reach a value of \$560M at chip level and \$4B at transceiver level in the 2025. In this context near-infrared (NIR) photodetectors (PDs) represent key devices but, unfortunately, Si is not provided of absorption over 1.1 microns. NIR Si-based PDs take conventionally advantage of germanium (Ge) integration on Si, however, due to a 4.3% lattice mismatch, the monolithic integration of Ge-based PDs with a Si-based electronic circuitry is not feasible. In order to make silicon suitable for detecting NIR wavelengths a chance is to take advantage of the internal photoemission effect (IPE). IPE occurs in a metal/semiconductor Schottky junction when the incident optical radiation is absorbed by the metal, and the photogenerated carriers are transferred into Si above the Schottky barrier. IPE has been widely used in platinum silicide (PtSi) Schottky barrier infrared CCD image sensors. However, the 512 x 512 focal plane array (FPA) based on PtSi require cryogenic temperature of 80 K [1] due the low signal-to-noise ratio. Replacing metal with graphene could be a disruptive idea for fabricating high-performance Si-based PDs and NIR imaging systems compatible with complementary metal oxide semiconductors (CMOS) technology. Indeed, increased IPE has been demonstrated in graphene/Si Schottky junctions, probably due to the two-dimensionality of the

material. Unfortunately, the efficiency of these PDs remains limited due to the low graphene absorption (only 2.3%). In order to increase the graphene optical absorption, we propose to incorporate the graphene/Si Schottky junction into a high-finesse Fabry-Pérot optical microcavity. Indeed, trapping of the NIR radiation inside the cavity allows to strongly increase the optical absorption of graphene and, consequently, the efficiency of the PDs. In the following the main results of the present work are summarized:

- Device concept has been defined and numerically investigated. Optimized structures show a 100% graphene absorption and performance comparable with the Ge technology. We have identified two possible configurations, highlighting the advantages and disadvantages for each;
- The fabrication flow-chart has been defined and the photolithographic masks designed for both configurations;
- The manufacturing process steps have been developed, testing the compatibility of the graphene layer with different etching solutions, gases and processes;
- Fabrication of some prototypes and preliminary electrical and electro-optical characterizations.

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## 2. STATE OF THE ART

PDs operating at 1550 nm can be fabricated by taking advantage of exotic materials, like indium gallium

arsenide (InGaAs) or Ge. While InGaAs is totally not compatible with CMOS technology, Ge can be grown starting from a Si substrate by the use of a buffer layer able to mitigate the lattice mismatch of 4.3%. Unfortunately, the fabrication of this buffer layer involves high thermal budget manufacturing processes, which prevent Ge to be monolithically integrated on Si. Therefore, Ge PDs are fabricated and then flip-chip mounted on Si-based transceivers [2], increasing production costs and hindering high-volume production. In particular, in the context of the NIR cameras, this reduces the pixel pitch (resolution) due to the assembly tolerance. This is why an all-Si approach should be preferred. The use of metal/Si junctions for detecting NIR light is not a new concept in literature. NIR focal plane array (FPA) based on 512 x 512 PtSi/p-Si pixels have been successfully monolithically integrated with an electronic Si circuitry [1]. However, these devices are characterized by a quantum efficiency <1% which hinders their application at room temperature. Since 2006, many strategies have been proposed for increasing the signal-to-noise ratio of these devices and for making them usable at room temperature, but the responsivities obtained for free-space PDs never exceeded 5mA/W [3]. The idea of replacing metal with graphene has recently opened up new perspectives. Unfortunately, even if increased IPE has been demonstrated in graphene/Si Schottky PDs, device efficiency is still limited by low graphene absorption (only 2.3%). In spite of the good responsivity of 20mA/W at 1550nm obtained using graphene [4], a further improvement is mandatory for making these devices usable in practical applications.

### 3. BREAKTHROUGH CHARACTER OF THE PROJECT

REVEAL aims to demonstrate that graphene can make Si a suitable material for the fabrication of low-cost PDs operating at NIR wavelengths. By the marriage between the most known material (silicon) with the most promising one (graphene), we aim to demonstrate for the first time that the high-performance NIR Si-based PDs could compare favourably with the well-established, but more expensive, technology based on III-V semiconductors or Ge. REVEAL will face two main challenges: 1) the increase of the optical graphene absorption at NIR wavelengths and 2) the integration of graphene with the CMOS technology. Point 1) has been faced by taking advantage of a high-finesse optical microcavity, able to strongly increase the graphene absorption and consequently the PD performances. Indeed, suspended graphene has a limited optical absorption of only 2.3% which has been proved to increase up to 8% when some low-finesse resonant structures have been adopted. REVEAL shows that graphene optical absorption can be increased to values very close to the theoretical limits, leading to efficiencies

comparable with Ge technology. Moreover, REVEAL will demonstrate high-speed PDs with bandwidth greater than 0.5 THz, delivering an impact on the new digital society, improving economic prosperity and a multitude of business, social and entertainment opportunities to its users.

Point 2) is a very challenging issue. In order to make graphene PDs fully compatible with CMOS technology, fabrication steps dedicated to graphene-related processes have been defined to be compatible with the back-end-of-line (BEOL) processes. This will open the door to the fabrication of NIR CMOS imaging systems monolithically integrated with the electronic circuitry, revolutionizing the field of NIR imagers as already the visible CMOS imaging systems did in the market of camcorder and digital cameras. In order to understand how this technology could be disruptive, it is sufficient to think to the smartphone market and to the possibility to integrate a NIR camera in any mobile phone, in the same way of visible camera. The keystone for the employment of these cameras for mass applications is to strongly reduce their cost. The technology developed by REVEAL will simplify the overall technology and reduce costs for the fabrication of photodetectors, making medium and high production volumes more affordable.

Our numerical simulations have clearly shown that the REVEAL PDs have the potentialities to overcome in performance the state-of-the-art of free-space Schottky PDs at 1550nm. Investigations are ongoing for matching experimental results with the theoretical predictions.

**Tab. 1.** Comparison with the main Schottky Si PDs reported in literature.

Main structures	Responsivity at 1550 nm (A/W)	Bandwidth
<i>Metal/Silicon [3]</i>	0.005	-
<i>Graphene/Silicon [4]</i>	0.02	MHz
<i>REVEAL (Fig. 3a)</i>	0.4	GHz

### 4. PROJECT RESULTS

The proposed PD is shown in Fig. 1: a graphene layer is placed in the middle of a cavity between crystalline Si (c-Si) and a hydrogenated amorphous Si (a-Si:H) layer. The three-layer system (a-Si:H/graphene/c-Si) is the optical cavity surrounded by a top and a bottom mirror. The bottom mirror shown in Fig. 1 could be either a distributed Bragg reflector (DBR) or a metallic reflector (MR). In the PD provided with DBR (DBR-PD) as bottom mirror, the charge carriers are collected transversally to the direction of the incoming light (yellow arrow), while for the PD with MR (MR-PD) the charge carriers can be collected longitudinally (white arrow), providing that MR works also as Ohmic contact.

In our simulations we have considered an ITO/Au bilayer as MR and some Si<sub>3</sub>N<sub>4</sub>/a-Si:H bilayers as DBR.

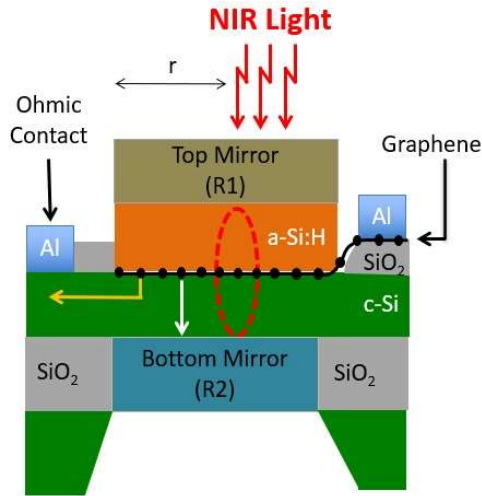


Fig. 1. Sketch of the proposed device.

Taking advantage of the Transfer Matrix Method (TMM) a graphene absorption of 93% can be achieved for DBR-PDs as shown in Fig.2. Numerical simulations show that the cavity could improve the graphene optical absorption with an increase larger than one order of magnitude compared to suspended graphene (whose absorption is only 2.3%). The parameters extracted from the numerical simulations able to optimize both the DBR- and the MR-PDs are reported in Table 2. The comparison of simulated responsivity, bandwidth and noise equivalent power, obtained for DBR- and MR-PDs, reported in Fig. 3(a)-(c) show that DBR-PDs are characterized by the highest responsivity of 0.4 A/W, the lowest NEP of 0.41 nW/cm $\sqrt{\text{Hz}}$ , as well as the highest selectivity. On the contrary, MR-PDs are characterized by the highest bandwidth and highest responsivity  $\times$  bandwidth product. Indeed, Fig. 3(b) shows that for a graphene circular area with radius of 70 $\mu\text{m}$ , the bandwidth is of 1 GHz for MR-PDs, and only 186 MHz for the DBR-PDs. From an experimental point of view, we have defined a fabrication flow-chart suitable to maintain full compatibility with Si technology, paying attention to full preservation of the graphene properties. The photolithographic masks have been designed and then fabricated. The device manufactured is shown in Fig. 3(d). The formation of the bottom mirror shown in Fig. 1 requires the etching of silicon from the back of a silicon-on-insulator (SOI) substrate, (we used a deep reactive ion etching (DRIE) process); then we removed the buried silicon dioxide in buffered HF solution and finally we deposited the ITO/Au MR on the back side of the membranes. Then, graphene is transferred on top of the Si chip and patterned, achieving an array of graphene PDs with different radius of the active area (one of them is shown in the inset of Fig. 3(e)). The step for having access to the back of the Si membrane is very challenging, because it is based on a large (up to 1 mm $^2$ ) ultrathin silicon membrane (220nm-thick). Several problems have been encountered due to the compressive stress of buried

oxide released at the edge of the membranes. These devices have been both electrically and electro-optically characterized. IV measurements show the expected rectifying behaviour as reported in Fig. 3(e). By a fitting procedure we have extracted some important electric parameters as the potential (Schottky) barrier of  $\Phi_B \sim 0.72\text{eV}$ , lower than photon energy at 1550 nm (0.8eV). Finally, we have performed electro-optical measurements proving that the structure is able to detect wavelengths around 1550 nm as shown in Fig. 3(f). Fig. 3(f) shows that the device responsivity increases by increasing the reverse voltage, a maximum responsivity of  $\sim 0.04\text{mA/W}$  at 1520nm has been experimentally achieved applying a bias of -4V. Ongoing work includes the fabrication of the whole structure reported in Fig. 1 and its electrical and electro-optical characterization. These results have been presented during two invited talks: ICTON 2020 (July 19-23, 2020) and Optical Microsystems 2019 (Sept. 9-11, Capri). Related results have been published on three international scientific journals (*Appl. Sci.* 2019, 9, 367; *J. of Eur. Opt. Soc.* RP, 2020, 16:6; *Micromachining* 2020, 11, 708) and presented to: Nanoinnovation 2019 (June 11-14, Rome, Talk), Graphene 2019 (June 25-28, 2019, Rome, Poster), and to the workshop “Wafer-scale integration of 2D materials” (Nov. 12-13, 2019, Aachen, Poster).

Tab. 2. Parameters extracted from the numerical simulations for achieving optimized PD performance.

Optimized parameters	Value
c-Si thickness	218.2 nm
a-Si:H thickness	216.2 nm
Top mirror reflectivity	0.976
Bottom mirror reflectivity	0.998

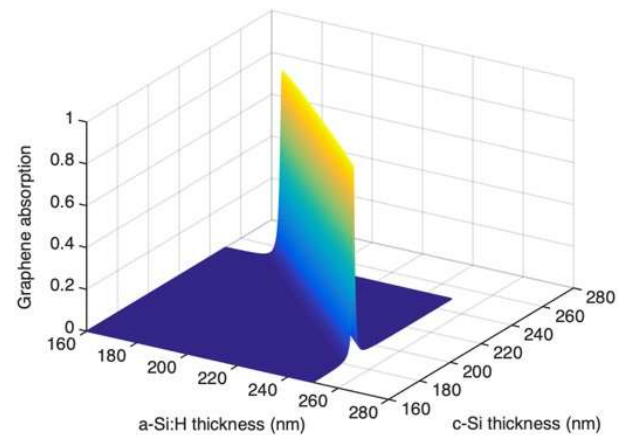
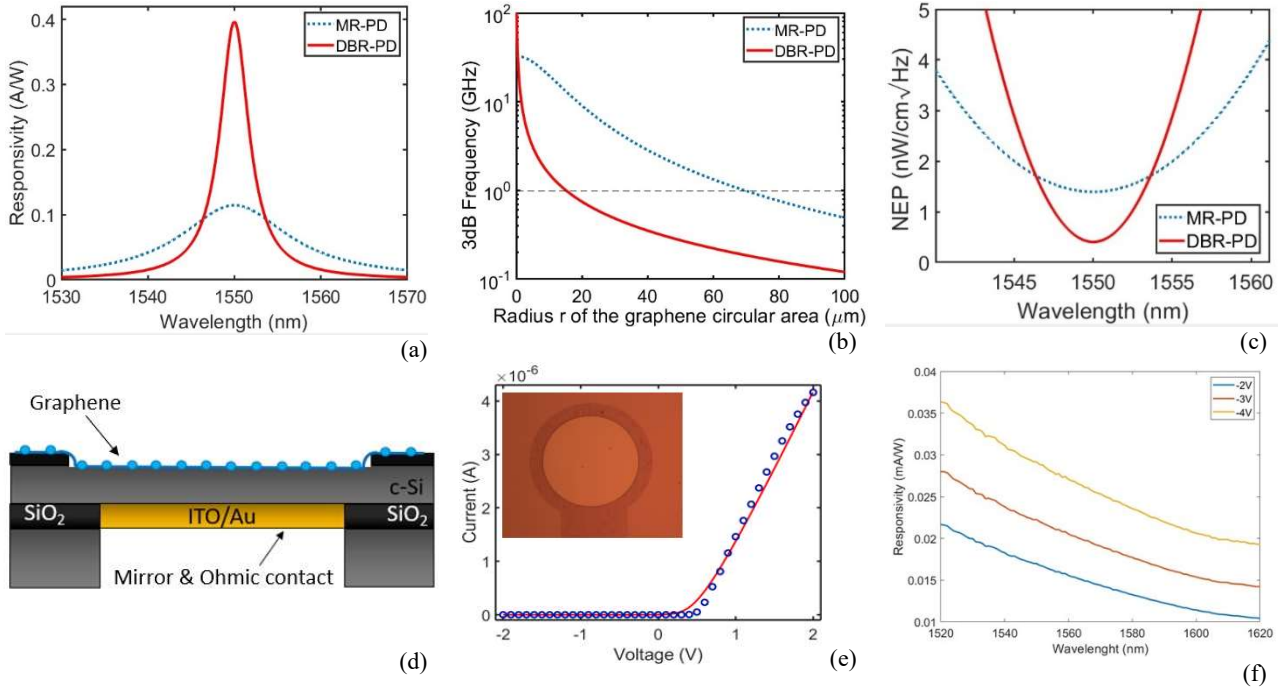


Fig. 2. Graphene absorption as function of both c-Si and a-Si:H thicknesses for the PD with a DBR as bottom mirror constituted by 5 pairs of Si $_3$ N $_4$ /a-Si:H.



**Fig. 3.** (a) Simulated responsivity (b) bandwidth and (c) NEP of the proposed PD provided with MR or DBR as bottom mirror. (d) sketch of the fabricated device. (e) I–V characteristic of Graphene/Si Schottky PD where experimental data and fit are shown. In the inset a top view of the device taken with optical microscope. (f) Experimental responsivity of Graphene/Si Schottky PD for different applied bias voltages.

## 5. FUTURE PROJECT VISION

### 5.1. Technology Scaling

Performance of the devices should be improved. This includes responsivity in the A/W range, bandwidth in the GHz range and noise equivalent power in the  $\text{pW}/\text{Hz}^{1/2}$  range. To reach this goal several aspects need to be considered: i) the manufacturing steps should be improved both in terms of repeatability and reliability; ii) the impact of the fabrication tolerances on the device performance should be optimized; iii) the Si substrates should be conveniently engineered; iv) the electronic circuitry driving the device should be designed and realized; v) lenses able to concentrate the NIR radiation onto the graphene absorber should be integrated.

### 5.2. Project Synergies and Outreach

For scaling to TRL 5-7 the following competencies should be added:

- i) Fabrication and development of high-reflectivity Si substrates based on a double SOI process;
- ii) Design of an electronic circuitry ranging from a simple noise filter to a more complex readout integrated circuit (ROIC);
- iii) Fabrication of the electronic circuitry described at the previous point ii);

iv) Design, realization and integration of lenses for the NIR optical coupling.

v) Realization of an efficient chip packaging.

It is worth noting that some of the aforementioned competencies could be taken from projects funded during ATTRACT Phase 1. Point iv) is compatible with OptoGlass3D project, while point ii) is compatible with DIBIS project. More important, carbon quantum dots/graphene hybrids materials developed in the BANDPASS project are very attractive, their employment as active layers on Si substrates should be exploited.

In order to ensure an effective communication and dissemination strategy, we propose:

- To prepare visual tools: project logo, a coordinated set of project tools for reports/papers, brochures, slide presentation etc;
- To publish brochures and leaflets to introduce the project, its objectives, and the foreseen outputs;
- To implement project web site containing a reserved area as well as public pages, to be used as showcase of the results;
- To use social media: Facebook and Twitter pages;
- To participate to targeted events.

### 5.3. Technology application and demonstration cases

Due to the huge increase in internet data traffic driven by the social network and video contents, both switching and interconnects of the existing data centre risk

becoming early a bottleneck. In this context, high-speed silicon PDs will have the potential to achieve a bandwidth greater than 0.5 THz delivering significant benefits on consumers. REVEAL will have an impact on the new digital society, helping to bring economic prosperity and a multitude of business, social and entertainment opportunities to its users. REVEAL will demonstrate monolithic high-resolution low-cost NIR CMOS imaging sensors to be employed in smartphone enabling real-time food and beverage inspection everywhere, also at the supermarket while shopping. Indeed, the NIR spectrum can interact with bonds as C-H, O-H and N-H which influence the quality of the food. In the same way pharmaceutical inspection could be addressed. NIR CMOS imaging systems demonstrated by REVEAL will revolutionize the field of NIR imagers, as visible CMOS imaging systems did in the market of camcorder and digital cameras, enabling their use in optical coherence tomography, biomedical imaging, passive night vision and night surveillance, automotive sensor systems, environment monitoring (LIDAR) and free-space optical communications in both terrestrial and space environment.

Our technology aims to involve Research Infrastructure (RI) communities in Europe for accomplishing the aforementioned chip packaging described at point v) of the section 5.2. Indeed, the Nanoscience Foundries and Fine Analysis – Europe (NFFA-Europe) RI could be included in the partnership. NFFA-Europe could also support the activity manufacture described at point iii).

#### 5.4. Technology commercialization

Main steps for reaching the first customer on the market:

- To draw a business model canvas (BNC) in order to clarify what is the product offered, who is the target market and how the business will get a profit.
- Prototyping and testing of a first product for testing the understanding of the customer's problem or need;
- Fabrication of an improved prototype for matching the value proposition with the customer's need (product market fit);
- Test selling.

At this stage, potential additional sources of financing could be business angels, entrepreneurs and crowdfunding platforms. Subsequently, the involvement of venture capital could lead to improve the product, to grow the customer base and to reach the break-even point (BEP).

#### 5.5. Envisioned risks

Critical risks and risk mitigation strategy (RMS):

- Limitation in device performance (Impact=medium – Likelihood=low). RMS: identification of causes and finding for alternatives;
- Difficulty in executing the dissemination plan (Impact=medium – Likelihood=low). RMS: close

and strong cooperation with the ATTRACT Consortium;

- Difficulty related to the consortium's heterogeneity (Impact=medium – Likelihood=low). RMS: increasing in internal reporting frequency and virtual meeting;
- Difficulty in attracting the interest from private investment stakeholders (Impact=high – Likelihood=low). RMS: clear and accurate dissemination strategy since the beginning.

#### 5.6. Liaison with Student Teams and Socio-Economic Study

MSc level students will be massively involved during ATTRACT Phase 2 and the following actions will be taken:

- A representative will be nominated among the partners for supporting and coordinating the student team;
- Periodic meeting will be planned for sharing suitable scientific references and material;
- It will be asked to the student team to choose a representative who will be able to attend to the partner meetings;
- The student team will be asked to propose innovative solutions on the main aspects of the project and to propose solutions if problem arise;
- The student team will be involved for disseminating the results of the project.

In order to support the socio-economic study of the experts, one idea could be to contribute to the creation of an accurate online and/or traditional survey which is a fast way to collect data helping to make better decisions.

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## 6. ACKNOWLEDGEMENT

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## 7. REFERENCES

- [1] Wang, W.-L. *et al.*, 1989, High fill factor 512 x 512 PtSi focal plane array, 1989 SPIE's 33rd Annual Technical Symposium, San Diego, CA, USA, 22 December 1989.
- [2] Narasimha, A. *et al.*, 2008, A 40-Gb/s QSFP Optoelectronic Transceiver in a 0.13 $\mu$ m CMOS Silicon-on-Insulator Technology, 2008 Optical Fiber Communications Conference, San Diego, CA, USA, 24-28 February 2008.
- [3] Desiatov, B. *et al.*, 2015. Plasmonic enhanced silicon pyramids for internal photoemission Schottky detectors in the near-infrared regime, *Optica*, 2(4): pp. 335-338.
- [4] Casalino, M. *et al.*, 2017. Vertically Illuminated, Resonant Cavity Enhanced, Graphene-Silicon Schottky Photodetectors, *ACS Nano*, 11(11): pp. 10955-10963.