Self-Powered Autonomous CMOS Camera SPACC

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ABSTRACT

The development of IoT requires sensors with a significant autonomy. Among them, cameras play a major roles for a lot of applications. Today some battery-powered cameras offer at the best several weeks/months of autonomy. The goal of the SPACC project is to design and manufacture a first prototype of a fully self-powered, low power, IoT camera embedding image processing.

Keywords: CMOS; autonomous; solar cells; camera; image processing; LoRa; IoT; low-power.

1. INTRODUCTION

The Self-Power Autonomous CMOS Camera (SPACC) is an IoT edge-computing device.

- Powered through solar cells
- No use of battery
- IoT: embarks low-power LoRaWAN communication

The first prototype is targeted at detecting car presence in a parking. It uses solar cells tuned for parking neon tubes and is designed from the ground up to an ultra-low-power device. The approach and prototype are very innovative:

- Thanks to its power supply autonomy and wireless transmission, the camera can be placed in locations that are difficult to access.
- The deployment of applications with many cameras is made economically possible thanks to the absence of infrastructure and maintenance costs.
- The absence of battery is interesting from an environmental point of view (no rare elements needed at production time, no waste at the end of product life).

DELTATEC and E-Peas built the prototype using the CAMEL sensor second version (improved of the baseline ersion of the imager) allowing to prove that an ultra-low-power autonomous camera can be built around the selected technology: E-peas image sensor, E-peas Power Management Integrated Circuit (PMIC), SemTech Lora Communication chip and low-power STM32L4 device allowing for low-power operation and decent processing power.

The prototype developed TRL3-TRL4 did not make use of the last E-peas image sensor, leading to pixels saturation complicating the image processing. Integrating the new E-Peas sensor would improve the performances

The results obtained are in line with the expectation of an acquisition, image processing and LoRaWAN communication every ~53 seconds with an illumination of 200 lux.

Fig. 1. SPACC First prototype

2. STATE OF THE ART

As mentioned in the introduction, the main challenge of the SPACC project is to design a camera that can be used to embed autonomous applications. The major challenge for DELTATEC is to reduce the power consumption of each component. In this section, we will review the state of the art of the PMIC and of the image sensor.

The system is supplied by light through a photovoltaic PV cell and a power manager, the AEM10941 from E-peas. See comparison with the competition (see **Tab** 1). The PMIC starts at the lowest input power which is 3 µW and 380 mW. The quiescent current is 400 nA whereas Analog Devices and Texas Instrument are at 510 nA and 488 nA. Those values become worse when we add the leakage current of the configuration resistors while the AEM10941 is I/O configurable. Finally, the AEM10941 has the lowest number of external components which allow a smaller footprint.

Tab 1: State of the art of PMIC – comparison of the different characteristics

Key Features	E-peas CIS	Texas Instrument	Analog Devices
Coldstart	3 µW @ 380 mV	15 µW @ 600 mV	6 µW @ 380 mV
MPPT configuration	I/O	Resistors	Resistors
Output type	LDOs	Buck	LDO
Quiescent current	400 nA	488 nA	510 nA
External components	7	14	17

The quality of an image sensor depends on two factors: its energy consumption (normalized per pixels per frame) and its image quality expressed in term of dynamic range (DR), signal to noise ratio (SNR) and fixed-pattern noise (FPN). **Tab. 2** shows the figure of merit of E-peas image sensor versus similar products from the competition.

Tab. 2. State of the art of low-power image sensor – comparison of the different characteristics

Key Features	E-peas CIS001	On Semi APTINA MT9V124	CSEM (ERGO imager)
Resolution	VGA	VGA	320x320
Active energy [pJ/pixel/frame]	165	~6000	683
Sleep power [µW]	0.1	44	/
DR [dB]	60 (linear) 90 (HDR)	58	120
SNR [dB]	45	33.4	/
FPN [%]	0.01	/	/
Max FPS	16	30	10
Bit depth	10	12	/

3. BREAKTHROUGH CHARACTER OF THE PROJECT

The development of IoT requires a broad range of sensors with a significant autonomy. Among them, cameras play a major role for a lot of applications. Today battery-powered cameras offer at the best several weeks/months of autonomy. Pre-processing in these devices is increasingly important to reduce the amount of data transferred on wireless links and doing it low-power is a key point.

The goal of the SPACC project was to design and manufacture a first prototype of a fully self-powered camera. It has been reached through combined elements:

- E-peas PMIC powers the board from solar-cells.
- E-peas sensor takes pictures at the fraction of the power needed by standard sensors.
- Direct use of LoRaWAN SemTech chip.
- STM32L4 low-power capabilities used to their best.
- Custom software and hardware tailored for lowest power consumption.

The SPACC is a camera that can perform basic image processing on the edge and send status information with low-power consumption as shown in **Tab. 3**. Note that attempt to send status information is only performed the status is relevant and if there is enough energy stored in the supercap.

Tab. 3. SPACC power consumption

Phase	Time (s)	Average Current (mA)	Power consumption (µWh)
Active	3.6	8.184	14.776
Sleep	50	0.0004	0.010

Those low power figures allow to perform acquisition, processing and communication every ~53 seconds. As the communication represents more than half of the power budget, acquisition and processing without communication could be performed every ~24 seconds.

4. PROJECT RESULTS

Unlike conventional imager, E-peas imager is based on a time-based architecture instead of high-speed ADC converters. The light information is encoded in the time domain rather than in the voltage. This allows to reduce drastically the voltage supplies of the circuit without suffering from a smaller SNR. **Error! Reference source not found.** shows the block diagram of the image sensor; it features a pixel array, some peripherals and a digital controller.

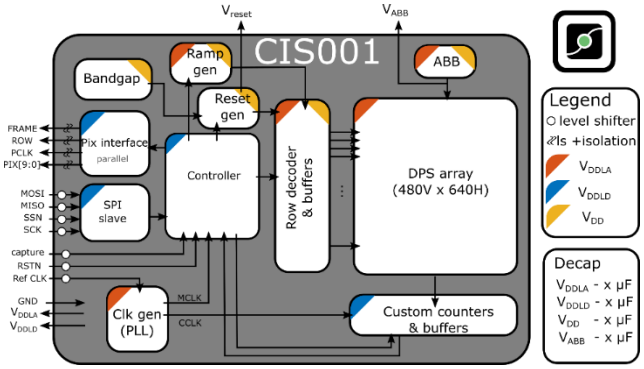

Fig. 2. schematic of the image sensor

Compared to the baseline version [1], multiple features have been added: high dynamic range (HDR), auto exposure, flip, edge map, region of interest, higher maximum frame rate, dead pixel correction and finally aggregation and decimation of pixels.

Error! Reference source not found. shows shows the results of the post-layout simulation regarding the image quality in comparison to the first version (CAMEL). The results are shown when we use the delta-reset-sample (DRS) technique to reduce the impact of the noise in linear mode and in HDR.

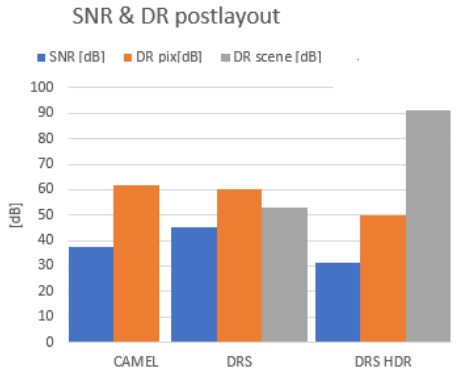

Fig.3 . results of the image quality (post-layout simulations)

Prevision of the power consumption based on the post layout simulation is shown in Tab 4. Compare to the first version power consumption remained constant despite the extra features and the higher frame rate.

Key Features	CAMEL	E-peas CIS
Idle	12µW	8.1 µW
Deep sleep	/	0.1 µW
DRS	177pJ/frame/pixel	1189 µW @ 16 fps 165 pJ/frame/pixel

Tab 4: Estimated power consumption of the image sensor

At every step, the design of the camera is taking in account the consumption in run mode as well as in sleep mode. The run mode has been split in major work phases:

- Boot and super cap level measurement
- Image acquisition
- Image processing
- Reference image update
- Remote communication

To reach that goal, every major hardware block can be programmatically powered on/off based on components that give the best compromise between on-mode static power dissipation and off-mode leakage currents. More generally, all paths between power supplies and the ground have been thoroughly checked.

The STM32L4S9 has been chosen for:

- Its good µA MHz specifications in run mode
- Its various sleep mode and power reduction features.
- Its internal RAM and Flash sizes allowing to avoid the use of an external SRAM and MRAM.

The software has been articulated around the work phases and all features of the CPU have been used to consume as few power as possible:

- Clock source selection
- System clock adjustment and Low Power Run/Sleep mode used whenever possible
- Regulator voltage scaling range

Due to planning constrains, the sensor used on board was not the latest version. This version was presenting interface drawbacks that imposed a high clock usage during the acquisition and longer duration. This leads to an important over-consumption that can be avoided when the latest sensor version is used.

The image is divided in predefined regions of interest, for which a cumulative histogram is processed allowing ROIs calibration to get each pixel value between to thresholds of the histogram. A significant change in the mean of ROIs pixels values define whether there is a change in the detection of a car.

The following table and figure shows the power consumption during the work phases and its associated time.

Tab. 5. SPACC detailed power consumption

Phase	Time (ms)	Average Current (mA)	Power Consumption (µWh)
Boot	5	1.359	0.003
Super cap check	19	2.759	0.026
Image acquisition	228	17.353	1.978
Image processing	374	25.440	4.757
LoRa communication	2985	5.367	8.010
Sleep	40000	0.0004	0.010

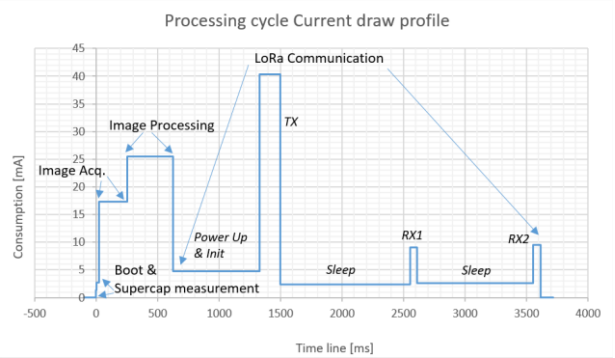

Fig. 4. SPACC detailed power consumption

5. FUTURE PROJECT VISION

5.1. Technology Scaling

The current application itself being car detection in a parking has the advantage to be easily testable and is a good use case in terms of processing. However, a lot of interesting technology domains have been studied in this project. Having a prototype being able to perform edge computing on a fully autonomous, self-powered IoT device establishes the base for many types of applications.

5.2. Project Synergies and Outreach

The consortium is now constituted by DELTATEC and E-Peas.

DELTATEC is an innovating design services company with competences in design of hardware, software, mechanics and manufacturing.

E-Peas produces energy harvesting power management system (photovoltaic, thermal, vibration, radio).

The collaboration of those two companies have been very enjoyable and both separated and common exposition of the prototype in industrial vision shows are under preparation.

A future consortium could be reinforced with additional organizations such as solar cells, thermo electric generator and mechanical harvester manufacturers.

5.3. Technology application and demonstration cases

The platform concepts are quite agnostic of the type of sensor and the energy source. The concept could be declined with other sources for the energy harvesting and other sensors as long as they are low power. The processing capability itself can be useful for a lot of applications that require periodic results.

The complete absence of maintenance needs as there is no battery to replace or recharge is a key point that would be more exploited in the next steps of the project. This is true for different domains. For example, this can be very interesting for several electronic devices used in health monitoring of elderly people at home. Indeed, the lack of the device maintenance by the monitored people themselves is a weakness and risk of the current solutions. Beside the platform itself, the processing algorithm development philosophy is also interesting for other power constrained domains whatever the reason (economic or technologic). On this aspect, DELTATEC is already working with other companies in the Earth Observation domain. Indeed, reducing the amount of data to transmit from a satellite by performing data analysis directly on the platform with a limited amount of power is a hot topic to better exploit the more and more complex science instruments embedded by the latest generation of satellite.

5.4. Technology commercialization

As a design house company DELTATEC doesn't not intend to commercialize the platform itself. The added value for DELTATEC lies in the innovative approaches that have been demonstrated in this use case. As explained in the previous subsection, we have already received interest for our ability to adapt standard processing algorithms to very low power platforms.

The SPACC prototype will be presented on the DELTATEC booths in the coming year (as soon as the international shows will be organized again after this COVID period).

5.5. Envisioned risks

The most difficult risk to mitigate at the beginning of a fully integrated low power system is the estimation of the processing power consumption. Tools exist for battery powered low power platform but doesn't take into consideration the specificities of the energy harvesting (like the intermittence of the energy source for example). The phase 2 should include the development of tools able to manage this kind of scenario.

6. ACKNOWLEDGEMENT

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7. REFERENCES

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