Single Photon Visible Light Image Sensors for Science and Technology

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ABSTRACT

A CMOS image sensor design based on multiple non-destructive signal sampling holds great promise in delivering single-photon sensitivity. Each signal measurement is statistically independent, and the electronic readout noise is reduced by averaging to a level where single photons are distinguished reliably. A pixel design using this method has been simulated and several layouts have been generated for a 180 nm CMOS image sensor process. The projected performance of our first prototype device indicates that single-photon imaging is achievable and will enable ground-breaking performance in many scientific and industrial imaging applications.

Keywords: Single photon imaging, CMOS image sensors.

1. INTRODUCTION

Single-photon (SP) imaging offers the ultimate performance in an imaging system due to its ability to capture and register each incoming photon. Its full strengths are most applicable in low light level conditions where every photon is valuable, such as in astronomy, adaptive optics, bio-imaging, quantum technologies, night vision, and surveillance. The demand for high performance SP sensors in the visible and near-infrared bands is growing and the list of applications is constantly expanding. SP imaging is only possible when electronic readout noise is negligible, and works by reconstructing images from multiple individual photons received in each pixel. This process is inherently noiseless and provides breakthrough performance compared to existing technology.

In this project we have investigated a concept for SP imaging in commercial complementary metal oxide semiconductor (CMOS) image sensor (CIS) technologies using averaging of multiple samples of the same optically generated signal. Because the signal measurements are non-destructive and nearly statistically independent, averaging reduces the readout noise by the square root of the number of samples. Single photons can be reliably detected with low error rate when sufficiently low readout noise has been achieved. Our image sensor achieves SP sensitivity through innovative combination of a photosensitive element with a multiple signal sampling technique, whilst allowing the sensor to be built using existing semiconductor manufacturing technology. This approach is unique in that it is the only single-photon imaging technique suitable for large-area sensors in a standard CMOS foundry process, opening the door for affordable single photon imaging in a variety of markets.

Our results show that SP imaging with silicon CIS using this principle is viable. We have calculated and simulated the expected readout noise performance using the parameters of a commercially available 180 nm manufacturing process. Several practical pixel designs have been created and simulated, while also considering any potential limitations arising from image lag, dark current and charge transfer efficiency. Our designs and simulations indicate that a megapixel-scale sensor operating at ~100 fps is feasible using present-day technology. The trade-off between readout speed and image sensor size allows many applications with diverse requirements to benefit from this development.

2. STATE OF THE ART

Two main methods for achieving SP sensitivity are used in semiconductor image sensors. In the first one, the photogenerated charge is amplified internally by a physical process before the conversion to voltage. In this way the signal is lifted well above the noise floor, allowing reliable SP detection. Typical examples are single-photon avalanche photodiodes (SPAD) and electron multiplying charge coupled devices (EMCCD), in which the primary photogenerated electron undergoes avalanche multiplication. Both can resolve single photons, however they suffer from shortcomings including high dark current rate and after-pulsing in SPADs [1] and spurious charge and excess noise [2] in EMCCDs. The EMCCDs also suffer from coincident losses in SP mode due to thresholding and effectively halving the detected quantum efficiency (QE) at high signals due to the excessive noise of the stochastic amplification process.

The second method involves reducing the readout noise of a sensor to a fraction of one electron root mean square (RMS) equivalent noise charge (ENC). Studies have shown [3] that for a practical single-photon imager with negligible error rate, the ENC must be below 0.15 e- RMS. Recent advances in CIS technology have reduced the readout noise significantly, and CIS with ENC below 0.3 e- RMS have been reported [4]-[6]. These developments are due to the increase of the conversion gain of the sensors above 200 µV/e- using special design and processing techniques, as well as by improvements to the noise performance of the readout transistors. Further noise improvements using those methods are certainly possible, however, the difficulties rapidly increase as the noise approaches the required level of 0.15 e- RMS.

Another related method using the “skipper” technique has recently demonstrated readout noise in CCDs reaching 0.068 e- RMS [7]. In skipper CCDs, the charge is transferred under a floating gate multiple times, measured after each transfer without affecting the charge, and the results are averaged. Although the noise performance is excellent, a major disadvantage of the multiple readouts is the greatly increased readout time, reaching several hours for CCDs. For a more practical device, the readout time must be reduced to at least a few seconds (e.g. for slow astronomical imaging), and to few milliseconds for applications requiring much higher frame rate (e.g. adaptive optics, bio-imaging etc.). In addition, a large concern for CCDs is that their future availability is uncertain as the number of CCD vendors is rapidly decreasing.

3. BREAKTHROUGH CHARACTER OF THE PROJECT

Our CMOS SP pixel design uses existing CIS processing technology and a novel combination of photosensitive, signal storage and readout elements, allowing us to overcome all of the limitations of the current state of the art SP imagers.

The breakthrough of this project lies in the further development of the skipper technique and its application to modern CISs. This approach can achieve sub-electron noise performance using designs and processes available today and offers high readout speed due to the inherent parallelism in CISs. In most CISs, an entire row of pixels is read out simultaneously, which reduces the readout time by three orders of magnitude compared to a sensor with a small number of outputs such as the CCD. In addition, the finer feature size in modern CIS allows the conversion gain of a floating gate readout circuitry to be much higher than in skipper CCDs. This enables substantial reduction of the readout noise in a single measurement, necessitating fewer signal samples to be averaged, and leading to an increase in the readout speed.

It is very desirable that the sensor can be operated in slow scan applications, such as in astronomy and biological imaging, in addition to the ability to achieve very fast frame rates in appropriately scaled sensors. Presently, only EMCCDs and skipper CCDs can be used in slow signal integrating mode, with SPADs excluded due to their very high dark current rate. At the same time, SP imagers for other applications need to be very fast in order to minimise photon pile-up when operated in photon-counting mode.

Unlike SPADs and EMCCDs, our device does not use avalanche electron multiplication and high voltages. In this way, the problems associated with spurious charge and excess noise are eliminated. The photosensitive element is a pinned photodiode (PPD), a mainstay of CIS technology due to its low dark current and the ability to store and transfer charge. Combining a PPD with a buried channel CCD-like structure that allows multiple charge transfers and sampling, offers the optimal architecture for SP imaging.

Table 1 outlines the main characteristics of the compared technologies in three categories. While not being able to match the sub-nanosecond response of SPADs, our development has distinct advantages in the other areas. The main competitor of our technology is the EMCCD.

Table 1. Single photon technology comparison.

Technology	Speed	Spurious signal	Signal integration
SPAD	Very fast	Poor	No
EMCCD	Fast	Fair	Yes
Skipper CCD	Very slow	Very good	Yes
This development	Fast	Excellent	Yes

4. PROJECT RESULTS

Readout noise

Based on the widely available 180 nm silicon processes, we have calculated the expected performance of the pixel implementation shown in Fig. 1. The pixel uses a floating sense gate SG1 to measure the signal non-destructively after charge transfer from the PPD. The charge is moved between SG1 and SG2 multiple times and re-sampled every time it is stored under SG1. The number of samples required to achieve readout noise below 0.15 e- RMS depends on the noise parameters of the readout chain and the time allocated to each sample. This time is the main limiting factor towards achieving high frame rate.

Fig. 2 shows the expected readout line rate taking into account the time for each sample and the number of averages required to achieve SP sensitivity. Since CISs are read out in a row-wise fashion, this metric is appropriate to estimate the frame rate for a sensor using this architecture. The data indicates that a sensor with one million pixels could achieve 30 readouts per second. This corresponds to ≈30000 rows/second at 1 MHz signal sample frequency and 34 averages to reach SP sensitivity. Frame rates above 100 fps are possible through increasing the conversion gain of the sense gate, the number of simultaneously read out rows, and the sampling frequency. Large format sensors with higher number of rows would tend to have lower readout rates, but this could be acceptable for slow scan applications such as astronomy.

Further increases in the frame rate and sensor size could be achieved by moving to CIS technology with finer feature size (such as 65 nm or 45 nm process) to reduce the parasitic capacitances, leading to a reduction of the read noise and the number of averaging samples.

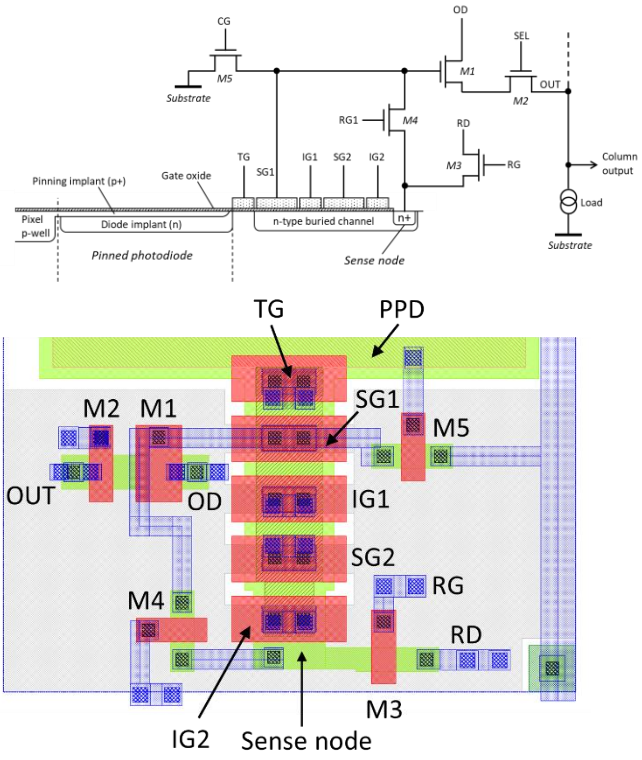

Fig. 1. Pixel schematic (top) and an example layout using 180 nm CIS process (bottom), showing the elements used in the multiple signal sampling and the readout circuitry [8]. Only the bottom part of the PPD is displayed.

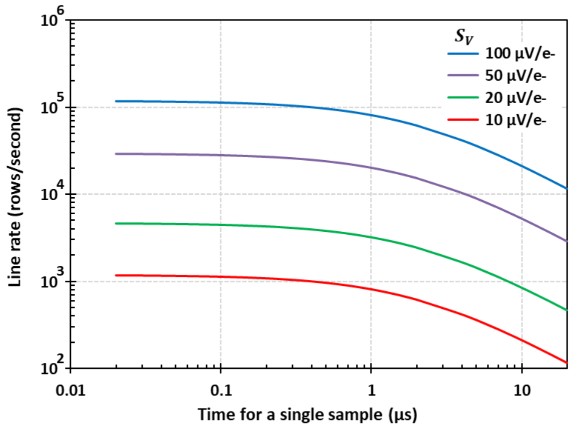

Fig. 2. Line rate for 0.15 e- RMS ENC for different conversion gains as a function of the time required for a single sample.

The proposed sensor architecture can serve the requirements for multiple sampling and signal averaging, is fully compatible with commercial CIS, and can re-use many existing design blocks, such as column amplifiers and analogue-to-digital convertors (ADC) using parallel dual-slope conversion.

The full description of the designs and the results from this project have been published in a peer-reviewed, open access paper [8].

5. FUTURE PROJECT VISION

5.1. Technology Scaling

We are currently designing a mega-pixel prototype with several different pixel variants, with a goal to complete the manufacture by the end of 2020. This work is intended to verify the operating principles and to benchmark actual performance against the simulations before embarking on the much larger task to develop a full-scale imager targeting specific applications.

Presently we estimate that the technology readiness level (TRL) is 2, and assuming a successful first prototype we can be at TRL 4 in the first half of 2021. This will eliminate some of the key risks associated with scaling up the technology towards a megapixel-sized sensor.

In ATTRACT Phase 2, we intend to team up with at least one end user and an experienced company with a strong background in developing commercial CMOS image sensors. The end deliverables are expected to be full size, functional SP imaging system prototypes including support electronics and software. The development is intended to demonstrate the technology via engineering models for the intended applications and is aiming at TRL 6.

5.2. Project Synergies and Outreach

Our consortium, presently comprising the Open University (UK) and the European Southern Observatory (ESO) (Germany) will need to expand substantially in order to further develop the technology.

In our preparations for ATTRACT Phase 2, we have already involved a company specialising in the design of high speed, ultra-low noise CMOS image sensors for industrial and scientific applications. The company is an established player in the field and has an excellent track record and knowledge of the market. The company will bring their intellectual property (IP) in high speed image sensor architectures and signal digitization to help us build the deliverables for the next phase.

ESO is the end user for two of the proposed applications – adaptive optics and large scientific imaging arrays. ESO is operating numerous adaptive optics systems and scientific astronomical imagers and spectrographs. The organization is actively developing new instruments that could use this technology for its forthcoming facilities, such as the Extremely Large Telescope (ELT). Some of the new and exciting science possible through ever fainter measurement regimes at ELT are the detection of biomarkers in atmospheres of nearby exoplanets and imaging the formation of planetary systems in Earth's neighbourhood. Many operational modes are fundamentally limited by detector noise; therefore, it is imperative to use imaging arrays that are essentially noiseless.

We are planning to involve one major EMCCD camera manufacturer as a route to developing our technology for life sciences and other applications outside astronomy. We will benefit from their excellent market and application knowledge, and established camera manufacturing and characterisation facilities. The collaboration is expected to shorten the time to market of our technology.

We are also investigating a collaboration with the team at Aalto University (Finland) (ATTRACT project #732: Superior gamma-detection and IR imaging via ALD-passivated germanium nanostructures) who are developing nanostructured anti-reflective coatings. When applied to silicon the coating improves the quantum efficiency to nearly 100% over the whole of the visible band. This can further improve the efficiency of our sensors because light reflection can be virtually eliminated.

In ATTRACT Phase 2, we plan to demonstrate our prototypes to the public. While we plan to publish scientific papers on our results, we can also assist the ATTRACT consortium in public dissemination of our results to a broader audience, for example through video demonstrations of our sensor in the lab, illustrating the "magic" of signal averaging, where a subject previously obscured behind noise is slowly revealed with more samples, and accompanied by a student-friendly mathematical explanation. These demonstrations can be coupled with real-world examples of the scientific applications of our sensor in fields such as astronomy and biology to highlight the breakthrough nature of our project and its benefits to humanity.

5.3. Technology application and demonstration cases

The applications of single photon imaging in the visible and near-infrared bands are diverse and constantly growing. Single photon imaging with negligible spurious and clock-induced signal is inherently noiseless and will provide a breakthrough performance when implemented in a large area CMOS image sensor.

We would develop technology demonstrators applicable to the following areas of SP imaging:

- Adaptive optics – targeting large scale facilities such as ELT with a megapixel-size sensor operated at several hundred readouts per second;
- Astronomy – direct exoplanet observation and lucky imaging for improved angular resolution;
- Life sciences - molecular fluorescence imaging applicable to real time detection of abnormal cell growth with multimodal biomarkers, fluorescent-guided surgery helping to better visualise the boundary between healthy and malignant tissue, requiring frame rate > 5fps;
- Spectroscopy with extremely faint astronomical sources such as exoplanets.

This diverse set of applications indicates that our development can benefit a large segment of the European and worldwide market for high performance CMOS imagers.

5.4. Technology commercialization

In order to create a commercial product, we need to scale up pixel prototypes into full-scale, functioning imaging arrays. This requires the following steps:

1) Sensor and pixel specification targeting a wide range of applications;
2) Detailed analysis of the characterisation results from the first prototype pixel demonstrator, and selecting the best design to go forward with;
3) Developing a commercial image sensor in two design cycles in collaboration with our industrial partner.

Additionally, commercialization into the diverse markets envisioned requires that the imaging arrays are fully integrated into cameras including cooling, readout electronics, and software. To achieve this, we will:

1) Engage with an established camera manufacturer (we are already in discussions) and with prospective users in the scientific and industrial communities from early sensor specification stage;
2) Work closely with our partners on prototype characterisation and camera integration throughout the design cycles;
3) Publicise widely our work with the aim to attract end users as customers.

For the ATTRACT Phase 2 we have already involved a company specialising in the design of high speed, ultra-low noise image sensors for industrial and scientific applications. The company has been operating for nearly 20 years and is expected to bring its rich expertise and existing customer base to the project.

Our existing consortium partner, ESO, would enable us to do first demonstration of the technology in adaptive optics and astronomy, while we plan to partner with an existing customer of our camera manufacturer for demonstration in the life sciences.

We believe that there is a robust commercial market for this product, however, significant funds are required to bring the technology from TRL2 to TRL6, at which point companies are willing to invest in integrating our imaging sensor into an existing product. Preliminary discussions with our partners indicate that the required funding to manufacture a full-scale SP image sensor at TRL6 will exceed €1M.

5.5. Envisioned risks

The main risk is in achieving the required performance using current 180 nm CMOS processes. Our first prototype pixel demonstrators, presently in design stage, are expected to retire many of the potential technological risks associated with achieving the required conversion gain and readout noise to allow SP sensitivity. Re-design and optimisation of the pixel layout and the manufacturing process are possible pending the outcome of this prototyping process. Any lessons learned will be taken onboard for ATTRACT Phase 2 and integrated into the final silicon layout.

5.6. Liaison with Student Teams and Socio-Economic Study

Collaboration with MSc student teams interested in using our technology for addressing societal challenges could work in synergy together with our prototype characterisation, in particular if the students are interested in carrying out a MSc thesis at ESO testing the prototype cameras and becoming familiar with the technology. Dr Elizabeth George and Dr Naidu Bezawada have supervised MSc theses in the past and would also do so for this project.

A more traditional approach would be a series of meetings between project members and the student teams, including demonstration of the technology and student-friendly lectures of how it works. Both Dr George and Dr Bezawada have extensive experience giving university lectures on detector technology throughout Europe.

To facilitate the socio-economic impact study, members of our project team would provide interviews to the team carrying out the study. The partnership's end user, ESO, would provide technical data comparing the performance of our SP CMOS technology to the current state of the art. Our commercial camera manufacturer could provide a comparative market study for our newly developed product based upon their current market penetration for competing technologies and forecasts for market growth.

6. ACKNOWLEDGEMENT

This project has received funding from the ATTRACT project funded by the EC under Grant Agreement 777222.

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